

Lab 2: Schematic Entry, Simulation, and Verification

Create an Inverter Schematic

Create an inverter with transistor values of $W=1.8\mu$ and the $L=0.6\mu$

- Create a new cellview
 - In the *Library Manager* window, select the *Labs* library and your *inverter* cell from Lab 1.
 - Go to *File -> New -> Cellview*
 - Select the tool which will select the cellview (*Composer - Schematic*)
 - The schematic tool should open
- Instance your devices.
 - type **i** to start the instance command
 - A separate window should appear
 - From the pulldown menu select *NCSU_Analog_Parts*
 - Choose the *N_Transistors* set
 - Choose the *nmos4* cell
 - Place the nFET by clicking on the canvas.
 - Get a *pmos4* from *P_Transistors*, and *vdd* and *gnd* from *Supply_Nets* .
 - Hit the escape key to get out of the instance command.
- Move your devices if you need to by selecting and dragging them or type **m** for move command
- Wire the circuit elements together
 - type **w** for the wire command or click on the red square ports and drag the mouse.
 - Double click if you want to end the wire unattached.
- Once the FETs are properly placed, choose a transistor and type **q** to look at it's properties. You may also modify a group of elements of the same type by selecting all of them and then *Apply to: all selected* button at the top of the properties window.
- In the properties window, set up your transistor size by entering
 - width: 1.8u
 - length: 0.6u
- Add an input and an output pin to your inverter.
 - type **p** to start the *add pin* command.
 - Enter all pin names separated by spaces (*Vin Vout*).
 - The pin names and type (i.e. input, output, inputOutput) must match what you entered for the layout design.
 - To place a pin simply move the cursor onto your schematic and click the button. You may not see an outline of the first pin that you place, that's ok, just click where you want it to go anyway and it will show up.
 - Connect the pins to the appropriate nodes with wires.
- Save your file.
 - Click on the *check and save* button on the left-hand side.
 - This also creates a netlist, which will be needed later when we compare the Layout versus the schematic (LVS)).
- **Print your schematic and have the instructor verify this portion of the lab.**

Create an Inverter Symbol

Turn the inverter schematic into a symbol.

- Go to *Design -> CreateCellview -> from cellview* (all defaults should be correct)
- Click OK and your symbol view will appear
- Now you have to change the symbol to something meaningful such as the inverter symbol
- There is a red outline around your entire symbol. This outline determines the mouse select area for your symbol. You may move and reshape this outline **but don't delete it.**
- You may also move the text within the square brackets, but **don't delete these either.**
- The tiny solid-red squares are the connection ports. You may move them, but **don't delete them.**
- The green lines are your actual symbol drawing. You may delete, move, change these as you like.
- Delete the green box and draw an inverter symbol. (go to *Add -> Shape -> Line*)
- Save your symbol (menu on left-hand side)
- Close the window (*window -> close*)
- **You don't need to print the symbol, but have the instructor verify this portion of the lab.**

Simulate the Inverter (Switch Level)

- You should always check your logic function before checking the timing.
- Create a new *schematic* cellview for your *RingOscillator* cell.
- Instantiate 49 copies of your new inverter symbol (use the array options of the instance command) and connect them in a chain, but **do not close the loop.**
- Add an input pin to the input of the first inverter and an output pin to the output of the last inverter. Name the pins whatever you like.
- Click on the *check and save* button on the left-hand side.
- Go to *Tools -> Simulation -> NC_Verilog* and a new window will pop up
 - In the new window go to *Commands -> Initialize Design*
 - Then *Commands -> Generate Netlist*
 - Then *Commands -> Edit Test Fixture.*
 - When the small window pops up click on the **Edit** button
 - Enter the following text for the stimulus module, but adjust for your input pin name:

```
initial
begin
    In = 1'b0;
    #200 $finish;
end

always #25 In = ~In;
```

- Save the file and close the text editor. If you have any syntax errors, the system will ask you if you want to fix them when you close the text editor.
- Click OK on the Edit Test Fixture window.
- Go to *Commands -> Simulate* in the NC-Verilog window, and two new windows will appear: **Design Browser 1 - SimVision** and **Console - SimVision**, .
 - Go to the *Design Browser* window and select the *test* cell

- You will then see your *top* cell appear below the *test* cell and all of the signals associated with the selected instance in the frame to the right
- Select which signals you want to display
- In the upper right corner of the Design Browser are several icons that choose different tools. Click on the black icon with the waveforms to send the signals to the waveform viewer. The waveform window should then pop up
- All of the simulator windows have a black “play button” on them. Clicking on this button in any window will run your simulation. The “rewind” button resets your simulation to begin again at “t=0”.
- If you want to add more signals to your display after you’ve already run your simulation: 1) send the signals to the waveform viewer using the Design Browser, 2) reset your simulation, and then 3) rerun your simulation.
- If you make a change to your schematic or Verilog code, you can rerun your simulation without closing the simulator and losing all of your display settings. In any simulator window go to *Simulation -> Reinvoke Simulator -> Yes*.
- **Display at least 4 different taps from the inverter chain in the Waveform Viewer including the input and output (a total of 6), and then get a printout of these waveforms.**
- Have your instructor verify this portion of the lab.

Simulate the Inverter (DC and transient characteristics)‘Go to the *RingOscillator* schematic window.

- Add your power supply
 - Instantiate a DC voltage source *Voltage Sources -> vdc*
 - Instantiate a vdd and gnd net and connect the DC supply to these nets
 - Set the DC supply to 5V through it’s properties window
- Add a pulsing voltage source (*Voltage Sources->vpulse*) to the input and a 15 fF capacitor (*RLC->cap*) to the output. You can use this source for both the DC and transient analysis.
 - For transient analysis:** Make *Voltage 1=0 V*, *Voltage 2=5 V*, the *rise and fall time* of the pulse = **0.1ns**, the *pulse width=25ns*, *period=50ns*, and *delay time=0*.
 - For DC analysis:** set the *DC Voltage* to **2.5 V**
- Start the simulator (*Tools -> Analog Environment*) from the schematic window.
 - In the simulator window:
 - Set up your transient analysis first (*Analysis->Choose*)
 - set the finish time to **200 ns**
 - Select the signals that you want to plot(*Outputs->to be plotted->select on schematic*). Click on the wires in the schematic to select voltages and the ports to select currents
Select the:
 - 1) input and output voltage and output current of the first inverter in the chain
 - 2) output voltage of the last inverter in the chain
 - 3) two voltages in the middle of the chain
 - Click on the green button to run the simulation.
 - A window should automatically appear with the curves drawn.
 - Zoom into a region of interest by right-click and dragging around that region
 - Use markers to take measurements
 - Place the first marker by going to *Marker->Place->Trace* and then click on the trace where you want the marker to go.

- Once placed you can select the marker and move it by clicking and dragging.
- Place the second marker using *Marker->Add Delta* and then click on the trace where you want to measure a difference from the first marker. Again you can move the second marker after it has been placed.
- Take the following measurements using the delta markers
 - the delay through a single inverter (50% to 50%) for a rising and falling transition
 - the delay through the entire chain (50% to 50%) from the input to output of the 48th inverter. **Do not include the last inverter.**
 - the rise and fall times of the output of the first inverter (10% to 90%)
- **Have your instructor verify this part of the lab.**
 - Now set up the DC Analysis (*Analysis->Choose*)
 - For the *Sweep Variable* choose **Component Parameter** then **Select Component**
 - Then select the vpulse voltage source in the schematic and then the **dc vdc “DC Voltage”** parameter
 - For the *Sweep Range* choose **Start-Stop** and enter **0** to **5**
 - Then choose a **Linear** sweep type and set the number of points to **5000**
 - Delete the transient analysis and then select for plotting only the input and output voltage of the first inverter
 - Run the simulation and look at the data.
 - Use the calculator to find the derivative of the voltage transfer curve and then measure and record the various inverter characteristics: V_{IL} , V_{IH} , V_{OL} , V_{OH} , and V_{TH}
 - In the waveform display window select Tools->Calculator
 - In the calculator window select the “dc” tab and then the “vdc” button below it.
 - Now click on the curve in the waveform window that represents the output of the first inverter. You should notice that the waveform field in the calculator window is update to reflect your selection.
 - Now choose the “deriv” calculation in the calculator.
 - In the pulldown menu just above the numbers in the calculator, select “New SubWin”
 - Then click on Eval, which is also just above the numbers.
 - If you did everything correctly, you should see a new subwindow that shows the derivative of your curve.
 - Print the DC voltage transfer curve of the inverter
- **Have the instructor verify this part of the lab.**

Extract your layout (create a schematic netlist from the layout)

- Open the layout view of the inverter (**not** RingOscillator) circuit
- click on *Verify ->Extract*.
 - in the Extract window, click on the *set switches* button
 - Choose “extract_parasitic_caps” and “keep_labels_in _extracted_view” (shift select to activate both)
 - Run the extractor and look for any errors in the main cadence window.
- Open the extracted view (go to the library manager and double click on the extracted view of the inverter).
- You should see your layers with schematic symbols placed on top. If you do not see the schematic symbols, you need to tell the editor to see multiple levels. Bring up the display options and change the display depth.

Layout versus Schematic (LVS - compare your netlists)

- Go back to the inverter layout window.
- Click on *Verify* -> *LVS*
 - In the LVS window, fill in the fields for the *Library*, *Cellname*, and *Cellview* or use the browse button.
 - be sure you compare your **schematic** with your **extracted** view
 - Hit OK and wait
 - you will see a window that says “LVS has succeeded”. This just means it is done, not correct!!
 - To see the results of the LVS, press the **output** button on the LVS window.
 - In the output window, look for the statement “The net-lists match” or “The net-lists failed to match”
 - If the netlists don’t match, you must find the error.
 - Click on the error display button and a new form will appear
 - Press the *Display* -> *First* button
 - The problem nodes will be highlighted on the schematic and the extracted view of the layout (note: you may need to open the schematic view)
 - Click on the *next* button to cycle through the problem nodes
- Fix your errors
 - if your problem is in the schematic, you MUST “check and save” the schematic to update the netlist
 - if your problem is in the layout, you MUST extract the layout again to update the netlist
- If you don’t have any errors, change one of the pin names in the schematic and then LVS again to see what the errors look like.
- **Have the instructor verify this portion of the lab.**

Informal Lab Report

Include the following sheet with the check points signed off by me. Be sure to include printouts of the schematic, the verilog simulation results, the DC simulation results, and transient curves in the final lab report. Also, please include answers to the following questions. Lab report is due at the BEGINNING of the next lab session.

Name: _____

Inverter Schematic check _____

Inverter Symbol check _____

Verilog Simulation _____

Transient Simulation Check _____

Single Inverter Delay (output rising) _____ (output falling) _____

Inverter Chain Delay (input rising) _____ (input falling) _____

Rise/Fall time: t_{rise} _____ t_{fall} _____

DC Simulation Check _____

V_{IH} _____ V_{IL} _____ V_{OH} _____ V_{OL} _____

V_{TH} _____

LVS of Inverter check _____

Questions and Calculations for Informal Lab Report

You may use this sheet or attach additional pieces of paper to answer the questions. Please attach an additional sheet of paper for the calculations. If you do the calculations in Maple, be sure to attach the Maple code showing the calculations and highlighting the answers.

1. Why is it important that we create symbols for our schematics?
2. Is the delay of the entire chain of inverters closer to 48 times the rising or falling delay of a single inverter? How can you get a closer estimate of the delay by using your measured rise and fall delays?

3. Why is the inverter threshold not 2.5 V? What consequence does this have on the logic path?

4. Explain the difference between the rise and fall times? How would you adjust the transistors to make the rise and fall times the same? If the rising and falling delays are different, why is the total propagation delay through the chain similar for both a rising and falling input? If the rise and fall times were equal, what would the delay of the inverter chain be?

5. What is the calculated value of the inverter threshold and how does it compare to the measured value? Use the MOSIS website to find the appropriate parameters for calculating the threshold. Explain some possible sources of error. See MOSIS test data file on ANGEL for parameter values.

6. What are the calculated values of the transient characteristics using the RC model and how do they compare to the measured values? Explain some possible sources of error. See MOSIS test data file on ANGEL for parameter values.