ECE 533: Programmable Logic Systems Design

Four credits — Spring 2004-05
ECE Department
Rose-Hulman Institute of Technology

Time and Location:

- Lecture: MTR 5 (11:45am – 12:35pm) in O-257
- Lab: W 4–6 (10:50am – 1:30pm) in B-200

Instructor: Dr. Ed Doering, D-211, 877-8977, CM 108, Ed.Doering@Rose-Hulman.edu. Office hours (TBA), other times available by appointment.

Course Web Pages:

- `http://www.rose-hulman.edu/~doering/ece533` (course-specific materials)
- `http://www.rose-hulman.edu/~doering/PLD_Oasis` (reference materials for labs)

Prerequisites: ECE 330 or ECE 333 or consent of instructor.

Catalog Description: Digital system-on-chip design techniques, including an advanced hardware description language, test-benches and verification, area and timing optimization, embedded microprocessors, and design for testing. Integral laboratory using contemporary CAD tools and FPGA devices.

Required Text: Smith, Michael J.S., *Application-Specific Integrated Circuits*, Addison-Wesley, 1997. ISBN 0-201-50022-1.

The text is also available on-line at `http://www.edacafe.com/books/ASIC/ASICs.php`

Grades: Grading is straight percentage as follows: 90% A, 80% B, 70% C, 60% D. The course score is based on the following percentages:

Mini-Exams	50 %
Lab Projects	25 %
Design Project	15 %
Homework	10 %

A passing course grade requires:

1. Overall mini-exam score at a passing level (at least 60%)
2. Completion of all lab projects
3. Completion of design project

Policies:

- Professional conduct is expected at all times.
- Mini-Exams:
  - Administered in class each Tuesday
  - Closed book and closed notes, no other aids permitted (calculators may be used, however)
  - 10 minutes duration.

  - Lowest score will be discarded when computing end-of-quarter grades.
  - Missed mini-exams may not be made up for any reason.
  - There is no final exam for this course.
- Homework:
  - Homework problems will be assigned periodically.
  - Use the standard homework format for the ECE Department.
- Lab:
  - Work in groups of two.
  - Lab write-ups are due at the beginning of the next lab period; late penalties apply afterwards.
  - Labs are group graded; limit your collaboration to your own lab group.
- Design Project:
  - Multi-week effort on an approved topic of your choice.
  - Project presentations will take place during 10th week.
  - Design project is group graded; limit your collaboration to your own lab group.
- Lab Equipment:
  - Each lab group will check out one (1) Digilent D2SB/DIO4/SIO1 FPGA prototyping board kit for the duration of the quarter.
  - All equipment must be returned in working condition no later than 4:00pm Friday of tenth week; course grades will be withheld until equipment is returned.
  - Students will be held financially responsible for any damage to the prototyping board kit.
- Laptop Computer:
  - Operating your computer in class for anything other than an approved course activity is not permitted.
  - Refrain from using your computer in a way that distracts others in class, e.g., surfing, e-mail, inappropriate images and screensavers, etc.

***RHIT Honor Code* Applied to this Course:**

- Work that you submit for individual grading must be entirely the result of your own effort. Unless clearly stated otherwise, all assigned work shall be interpreted as "individually graded."
- Work that you submit for group grading is a result of equally shared effort.
- Avoid any form of or the appearance of any form of academic misconduct, which will result in a minimum penalty of zero credit for the work in question, and may result in a maximum penalty of a failing course grade. Examples include:
  - Plagiarism (submitting the work or ideas of others as if they were your own)
  - Receiving assistance on quizzes or exams
  - Transmitting the content of or answers to quizzes or exams to others

Tentative Schedule

Day	Date	Topic	Reading
1-1	M 3/7	Introduction and course overview	—
	_____	*Alternative implementation technologies*	
1-2	T 3/8	ASIC categories, design economics	Ch 1.1–8
1-3	R 3/10	Design economics (cont'd)	
	_____	*Advanced Verilog techniques*	
2-1	M 3/14	Refresher: combinational circuits	Ch 11.1–3
2-2	T 3/15	Refresher: sequential circuits	
2-3	R 3/17	Finite state machines	
3-1	M 3/21	Hierarchy and instantiation	Ch 11.4
3-2	T 3/22	Functions and tasks	Ch 11.7
3-3	R 3/24	Testbenches: input stimulus	Ch 11.5–6, 8
4-1	M 3/28	Testbenches: external emulation	Ch 11.9–12
4-2	T 3/29	Testbenches: response comparator	Ch 11.13–14
	_____	*Space and speed optimization*	
4-3	R 3/31	Efficient synthesis guidelines	Ch 12.1–2
5-1	M 4/11	Space optimization styles	Ch 12.3–5
5-2	T 4/12	FSM space optimization	Ch 12.7
5-3	R 4/14	LFSR counter, timing issues, prescalers	Ch 12.8
6-1	M 4/18	Speed optimization: pipelining	Ch 12.9–10
6-2	T 4/19	Speed optimization: timing constraints	Ch 12.11
6-3	R 4/21	Timing verification	Ch 12.12–13
7-1	M 4/25	Embedded processor cores	
7-2	T 4/26	Memory mapping interface	
7-3	R 4/28	Intellectual property (IP) cores	
	_____	*FPGA hardware and architecture*	
8-1	M 5/2	Programming technologies	Ch 4
8-2	T 5/3	Programmable logic cells	Ch 5
8-3	R 5/5	Programmable I/O cells	Ch 6
9-1	M 5/9	Clock distribution, DLLs	
9-2	T 5/10	Advanced architectures	
9-3	R 5/12	Advanced architectures	
	_____	*Applications*	
10-1	M 5/16	Reconfigurable computing	
10-2	T 5/17	Real-time signal processing	
	W 5/18	***Design Project Presentations***	
10-3	R 5/19	High-speed serial links	