Course Plan for ECE 533

Vision

A "vision statement" describes the best possible results that could be achieved.

Graduates of ECE 533 will contribute significantly to the development of new semiconductor-based information processing systems.

Mission

A "mission statement" describes what is done to work toward the vision.

ECE533 encourages and assists students as they learn the fundamentals of system-on-chip (SoC) design as implemented on programmable logic devices.

Guiding Principles

"Guiding principles" articulate beliefs and assumptions that influence the way the mission will be carried out.

1. All class members are self-motivated learners with a strong drive to excel
2. All class members exhibit the professionalism of degree-holding engineers
3. Students should have freedom to chart their own learning path within the guidelines set by the course structure
4. Hands-on design experience with modern EDA (electronic design automation) tools and hardware is vital to learning
5. Honesty, hard work, timeliness, and desire to learn are important to all class members

Learning Goals

What does the instructor want you to know, to think, and to be able to do after you invest your time and energy into this course?

1. Appreciate the challenges of creating mega-gate system-on-chip designs that work correctly the first time
2. Combine diverse elements into a system-on-chip architecture and hardware implementation that meets space, timing, and total development time and cost constraints
3. Incorporate design-for-reuse methodologies in all your design work
4. Demonstrate facility for research and independent learning
5. Care deeply about designing and building reliable and high-quality systems
6. Schedule and conduct a small-scale system-on-chip design activity that includes research, product specifications, architecture design, implementation, and testing

Learning Objectives

Specific, measurable behaviors that indicate that the goals have been met.

1. Demonstrate ability to design the architecture of a small-scale system-on-chip using the following elements:
   (a) self-designed IP
   (b) third-party IP
   (c) target-specific soft and hard IP
   (d) microcontroller or microprocessor core
   (e) software program
2. Demonstrate ability to carry out the complete system-on-chip implementation process, including:
   (a) create specifications that properly state functionality and space/timing constraints
   (b) create architecture that satisfies functional specifications
   (c) enter HDL design with appropriate style to optimize space and timing constraints
   (d) develop testbench that includes high-level control constructs and external system emulation
   (e) perform function verification using a behavioral simulator
   (f) interpret synthesis and place-and-route reports to verify that design meets space and timing constraints
   (g) perform timing verification using a behavioral simulator with post-layout timing
   (h) verify in-system operation of the system-on-chip
3. State the key distinguishing characteristics of ASICS, e.g., full-custom, semicustom, standard cell, antifuse FPGA, SRAM-based FPGA
4. Evaluate the sutability of each of the previously-defined ASIC categories for a given application
5. Describe standard design-for-test methodologies
6. Discuss economics of ASIC-based systems
7. Present results of project work in written and oral format
8. Select appropriate CAD tools and learn new tools to implement your own small-scale system-on-chip designs