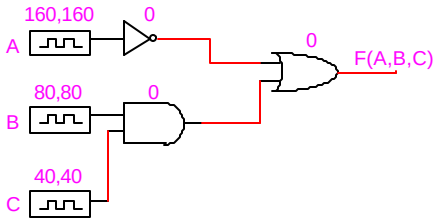
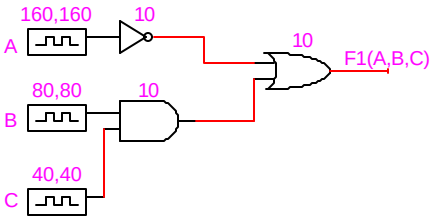
**Name** _____ **Box** _____ **Due date:** **Mon. March 19**

## ECE130 Homework #6 (gate delay & 7400 chips) Spring 2001

1. *Two implementations of a logic function F(A,B,C) are shown below. One uses gates that have no delay and the other uses gates with 10-unit time delay each.*

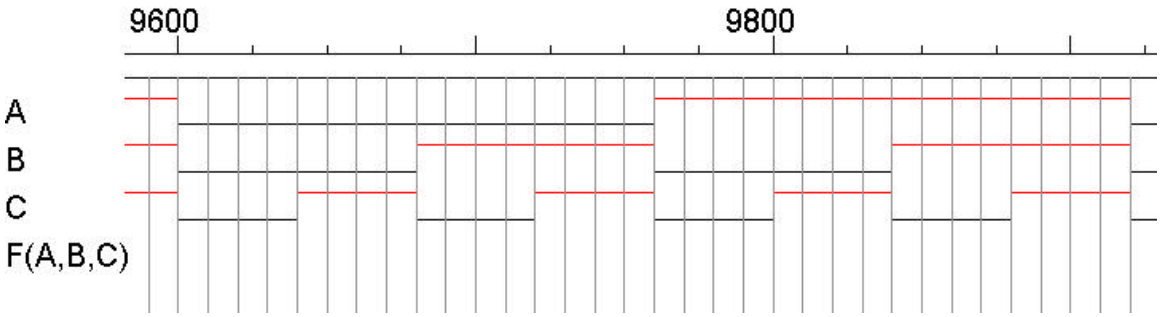



(A)

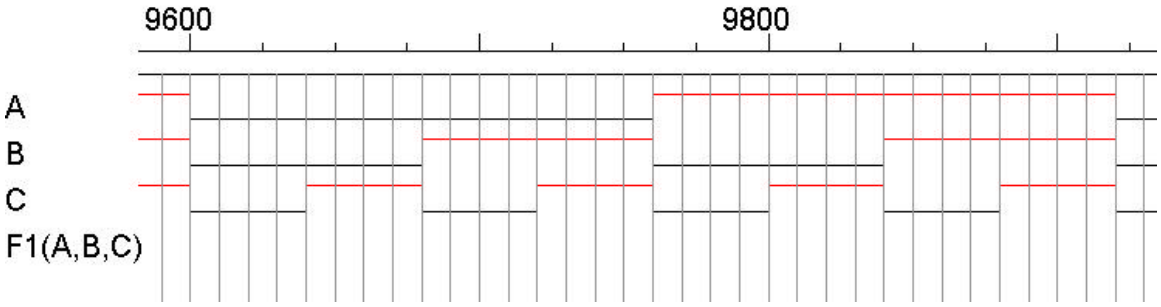



(B)

*(A) Draw the output waveform of F(A,B,C) with zero time delay gates for all the input combinations. The grid interval is 10 time units.*




*(B) Draw the output waveform of F1(A,B,C) with 10-unit time delay gates for all the input combinations. The grid interval is 10 time units.*




2. *Implement and simulate a full adder (addend, augment and carry-in) with standard 74 series of chips. The 74 series of chips are in device library 7400devs.clf that comes with LogicWorks 4. Assuming zero delay, attach a printout of your circuit schematic and waveforms with your homework submission. Verify the truth table on the waveforms by filling in the truth table on the waveforms. (Here are some relevant chips: 74__04 Inverters, 74__08 AND gates, 74__32 OR gates.)*