Winter 2015-2016 CSSE 232

Milestone 2

Team:	Date:
Design document:	
List of components	
List of input, output, and control signals (with bit counts)	
Description of each component input/output/control bits	
RTL for each instruction or type	
Tests for RTL	
Note of any changes to previous work	
Other:	
Journal	
Status memo	

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