CSSE 232 – Computer Architecture I
Rose-Hulman Institute of Technology
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Performance Examples

Example 1

Consider two different implementations, M1 and M2, of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 400 MHz, and M2 has a clock rate of 200 MHz. The average number of cycles for each intruction class on M1 and M2 is given in the following table:

Inst. Class	M1 CPI	M2 CPI	C1 Freq	C2 Freq	3P Freq
A	4	2	0.3	0.3	0.5
B	6	4	0.5	0.2	0.3
C	8	3	0.2	0.5	0.2

The table also contains a summary of how three different compilers use the instruction set. C1 is a compiler produced by the makers of M1, C2 is a compiler produced by the makers of M2, and the other compiler is a third-party product. Assume that each compiler uses the same number of instructions for a given program, but that the instruction mix is as described in the table.

1. Using C1 on both M1 and M2, how much faster can the makers of M1 claim that M1 is compared with M2?
2. Using C2 on both M2 and M1, how much faster can the makers of M2 claim that M2 is compared with M1?
3. If you purchase M1, which compiler would you use?
4. If you purchase M2, which compliler would you use?
5. Which machine would you purchase if we assume that all other criteria are identical, including cost?

Example 2

Consider an architecture that is similar to MIPS except that it supprts update addressing for data transfer instructions. Update addressing allows a data transfer instruction to "update" the address of the data transfer for "free" during the data transfer, potentially eliminating the need for an arithmetic instruction after the data transfer is complete. For example, if we load a value from memory and then load the value in the next memory location. The unmodified MIPS architecture would require 2 data transfer and 1 arithmetic instruction to accomplish. The modified architecture (i.e. supporting update addressing) would only require 2 data transfer instructions. For a given program the modified and modified architectures have the instruction frequencies and cycles per instruction shown in the table below. If 25% of the data transfer instructions can take advantage of update addressing which will be faster on this program, the modified MIPS architecture or the unmodified architecture? How much faster? The modified architecture has its cycle time increased by 10% in order to accommodate the new instruction.

Instruction	freq	Cycles
Arithmetic	24%	1.0
Data transfer	36%	1.4
Logical	18%	1.0
Branch	18%	1.7
Jump	3%	1.2

Example 3

We are interested in two implementations of a machine, one with and one without special floating-point hardware. Consider a program, P, with the follwing mix of operations:

floating-point multiply	10%
floating-point add	15%
floating-point divide	5%
integer instructions	70%

Machine MFP (Machine with Floating Point) has floating-point hardware and can therefore implement the floating-point operations directly. It requires the following number of clock cycles for each instruction class:

floating-point multiply	6
floating-point add	4
floating-point divide	20
integer instructions	2

Machine MNFP (Machine with No Floating Point) has no floating-point hardware and so must emulate the floating-point operations using integer instructions. The integer instructions all take 2 clock cycles. The numberof integer instructions needed to implement each of the floating-point operations is as follows:

floating-point multiply	30
floating-point add	20
floating-point divide	50
integer instructions	2

Both machines have a clock rate of 1000 MHz. Find the native MIPS ratings for both machines.

Example 4

Your current processor design supports a multiply instruction take 12 cycles and accounts for 15% of the instructions in a typical program. The other 85% of the instructions require an average of 4 cycles for each instruction. Your hardware engineering team has indicated that it would be possible to reduce the number of cycles required for multiplication to 8, but this would require a 20% increase in the cycle time. Nothing else would be affected by the change. Should they proceed with the modification?