## CSSE132

## Introduction to Computer Systems

11 : Basic computational structures
March 20, 2013

## Today: Basic computational structures

- Helpful structures
- Decoder/encoder
- Multiplexor/demultiplexor
- Sign extender
- ALU
- ALU control
- Zero detector
- Set less than


## Decoder/encoder

- Outputs unique signal based on input
- Inputs: state of systems
- Output: unique representative code
- 2 inputs $=2^{2}$ outputs
- Encoder reverses the process



## Multiplexor

- Select single data stream from multiple channels
- Multiple data inputs
- Single data output
- Control S selects single data stream


| $\mathrm{S}_{2}$ | $\mathrm{~S}_{1}$ | $\mathrm{~S}_{0}$ | Y |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | $\mathrm{D}_{0}$ |
| 0 | 0 | 1 | $\mathrm{D}_{1}$ |
| 0 | 1 | 0 | $\mathrm{D}_{2}$ |
| 0 | 1 | 1 | $\mathrm{D}_{3}$ |
| 1 | 0 | 0 | $\mathrm{D}_{4}$ |
| 1 | 0 | 1 | $\mathrm{D}_{5}$ |
| 1 | 1 | 0 | $\mathrm{D}_{6}$ |
| 1 | 1 | 1 | $\mathrm{D}_{7}$ |

## Demultiplexor

- Outputs data to one of multiple data channels
- Single data input
- Multiple data outputs
- Control S selects data output


| $\mathrm{S}_{1}$ | $\mathrm{~S}_{0}$ | Data | $\mathrm{D}_{0}$ | $\mathrm{D}_{1}$ | $\mathrm{D}_{2}$ | $\mathrm{D}_{3}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

## Sign extender

■ CPUs work with signed numbers

- Word size or smaller
- Often need to convert to word size
- Need to duplicate (extend) sign bit
- Preserves original number in larger container
- How to do this?


## Sign extender

- CPUs work with signed numbers
- Word size or smaller
- Often need to convert to word size
- Need to duplicate (extend) sign bit
- Preserves original number in larger container
- How to do this?
- Just connect MSB input to sign extend bits!
- Only need wires


## ALU

- Arithmetic Logic Unit
- Responsible for all computations in computer
- Supported operations
- AND
- OR
- Add
- Subtract
- Is less than
- Is equal
- Others: NOT, NOR, NAND...
- Design is similar to adder
- Start with 1 bit ALU, expand


## 1 bit ALU

- Start with AND and OR operations
- Inputs A and B
- Select operation by control signal OP
- Single output R

■ Hint: a multiplexor will help!

- Op 0 = AND
- Op 1 = OR


## 1 bit ALU

- Start with AND and OR operations
- Inputs A and B
- Select operation by control signal OP
- Single output R



## 1 bit ALU

- Add in ADD
- We'll use a full adder
- Inputs A, B, Cin
- Outputs $\mathrm{S}, \mathrm{C}_{\text {out }}$
- $S=A B^{\prime} C_{\text {in }}{ }^{\prime}+A^{\prime} B C_{\text {in }}{ }^{\prime}+A^{\prime} B^{\prime} C_{\text {in }}+A B C_{\text {in }}$
- $C_{\text {out }}=A B+B C_{\text {in }}+A C_{\text {in }}$


## 1 bit ALU

- Add in ADD
- We'll use a full adder
- Inputs A, B, C in
- Outputs $\mathrm{S}, \mathrm{C}_{\text {out }}$
- $S=A B^{\prime} C_{\text {in }}{ }^{\prime}+A^{\prime} B C_{i n}{ }^{\prime}+A^{\prime} B^{\prime} C_{i n}+A B C_{i n}$
- $C_{\text {out }}=A B+B C_{\text {in }}+A C_{\text {in }}$
- Need to expand mux



## Wider ALU

- Can link 1 bit ALUs together to form large ALU
- 32 bit example



## Subtract

■ Given that 1 bit ALUs form larger ALUs, implement subtract

- Remember Two's complement!
- $-x=\left(\sim^{x}\right)+1$
- What do we need?



## Subtract

- Given that 1 bit ALUs form larger ALUs, implement subtract
- Remember Two's complement!
- $-x=\left(\sim^{x}\right)+1$
- What do we need?
- Invert B or A
- Add 1 to LSB



## Subtract

- Invert B
- Still need to use adder, so don't expand mux (keep using + op)
- Add control line to select inverted B



## Subtract

- Add 1 to LSB
- If operation is subtract
- Set LSB carry in to 1
- Set ALU op to +
- This incredible convenience is why most computers use two's complement



## Equal

■ Add 1bit 'zero' output to ALU

- Set to 1 when $A$ and $B$ are equal
- How to do?
- Subtract A and B
- If all bits are 0 , must be equal!
- OR all bits
- Invert result


## Other operations

- Could add more operations
- NOR (invert A)
- Shifting (special hardware)
- Many others...


## ALU with NOR support



## Set less than

- If $\mathbf{A}<\boldsymbol{B}$
- R = 0x00... 01
- If $\operatorname{not} \mathrm{A}<\mathrm{B}$ (i.e. $\mathrm{A}>=\mathrm{B})$
- $\mathrm{R}=0 \times 00 . . .00$

■ How to do this?

- Subtract is useful
- Sign-bit (MSB) is useful
- Need to expand mux for new operation


## Set less than

- If $A<B$
- $\mathrm{R}=0 \times 00 . . .01$
- If $\operatorname{not} \mathrm{A}<\mathrm{B}$ (i.e. $\mathrm{A}>=\mathrm{B}$ )
- $\mathrm{R}=0 \times 00 . . .00$

■ How to do this?

- Set LSB to MSB (sign bit)
- Output 0 for all other bits


## Set less than

- If $\mathbf{A}<\mathbf{B}$
- R = 0x00... 01
- If $\operatorname{not} \mathrm{A}<\mathrm{B}$ (i.e. $\mathrm{A}>=\mathrm{B}$ )
- $\mathrm{R}=0 \times 00 . . .00$
- How to do this?
- Add new input ‘less’
- Can 0 to result mux
- Add new output 'set' to MSB ALU
- Output MSB result
- Use later



## Set less than

- If $\mathbf{A}<\boldsymbol{B}$
- R = 0x00... 01
- If $\operatorname{not} \mathrm{A}<\mathrm{B}$ (i.e. $\mathrm{A}>=\mathrm{B}$ )
- $\mathrm{R}=0 \times 00 . . .00$
- How to do this?
- Set ALUs to subtract
- MSB 'set' is now sign bit
- Pass MSB 'set' to LSB 'less'
- Set all other 'less' to 0



## Set less than

- If $A<B$
- R = 0x00... 01
- If $\operatorname{not} A<B$ (i.e. $A>=B)$
- $\mathrm{R}=0 \times 00 . . .00$
- Result
- Subtract results in < 0
- Sign bit of 1 is sent to LSB
- Subtract results in >=0
- Sign bit of 0 is sent to LSB
- All other bits set to 0


