

Homework 5 **(Control Unit and ALU design)** **Maximum points: 45 points**

Directions

This assignment is due Monday, Oct. 31st. Submit your solutions on a separate sheet of paper.

Learning Objectives

In the process of completing this homework assignment, students will develop their abilities to

- Design control units to support machine language instruction sets by applying combinational and sequential digital logic design principles.
- Design digital logic circuits for computer arithmetic.
- Predict the qualitative effect on clock cycle time of modifications to the design of digital logic circuits

General Instructions

- For the micro-programming problems, you do not have to re-produce the micro-program in Figure 5.7.3. Assume that that part of the micro-program already exists and write down only the new micro-instructions that are required. Also, if you create any new values for the fields or new fields, clearly specify what each new value/field denotes.
- Submit your answers on a separate sheet of paper.
- The state diagram for the FSM representation of the control unit (Figure 5.38) is provided on the class website.
- Figures 5.7.2 and 5.7.3 that deal with micro-programming are provided on the class website.
- Figures for the 32-bit adder are also provided on the class website. Make modifications on these figures for Problem 4.

Problems

1. [15 points] Figure 5.7.3 in Hennessy and Patterson (the CD actually), shows the microprogram for the control unit of the MIPS architecture that can handle `lw`, `sw`, `beq`, `j` and R-type instructions. Add microcode to this program to implement the following MIPS instructions:

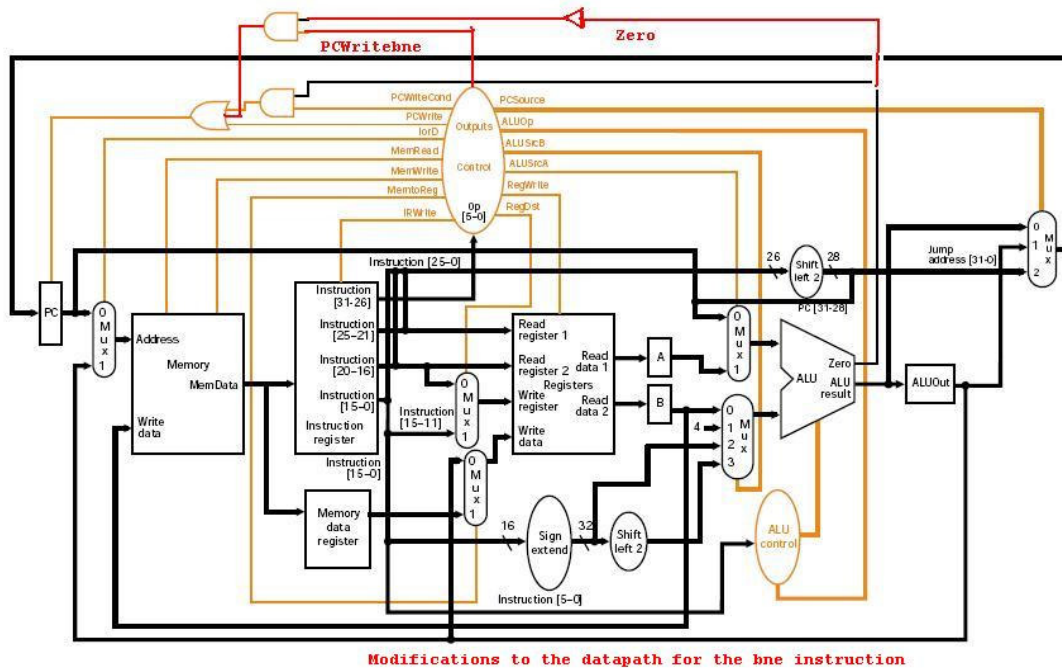
- a. `bne`
- b. `jr`
- c. `lui`

Figure 5.7.2 on the CD lists the control fields and their values that the microprogram uses.

The RTL for the bne is provided below:

1. $PC = PC + 4$; $IR = Mem[PC]$
2. $A = Reg[IR[25:21]]$; $B = Reg[IR[20:16]]$;
 $ALUOut = PC + (SE[IR[15:0]] \ll 2)$;
 If $(IR[31:26] == 5)$ then
3. If $(A - B \neq 0)$ $PC = ALUOut$

The modified datapath for bne is below:



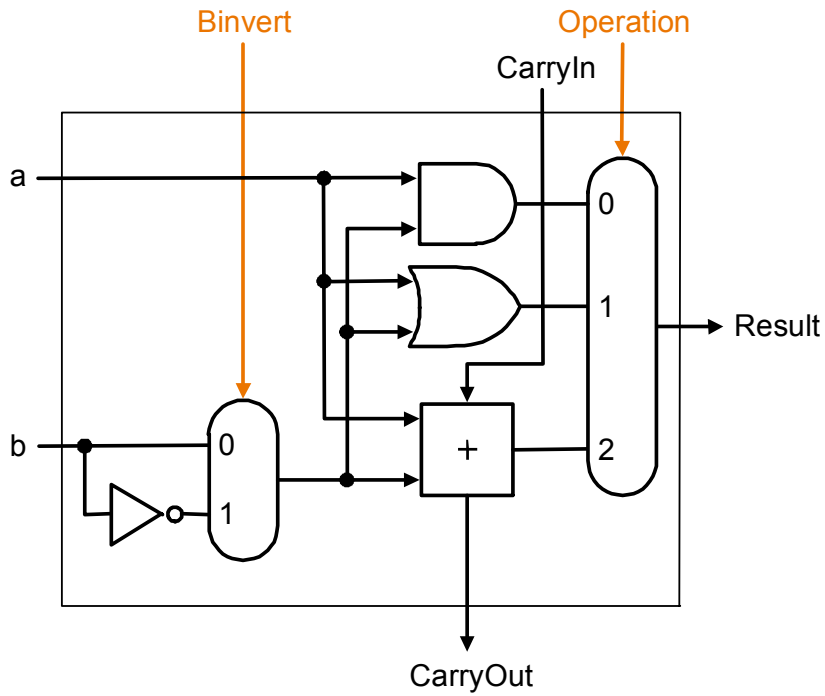
The RTL and the modified datapaths for the jr and lui instructions are available as solutions to HW3 and HW4. You must use the provided solutions for questions 1 and 2 on this homework.

2. [15 points] For each of the problems below, modify the textbook's multi-cycle control (Figure 5.38 on page 345) to implement the indicated MIPS instruction. Use a separate printout for each of the instructions. A copy of Figure 5.38 is provided on the class website.

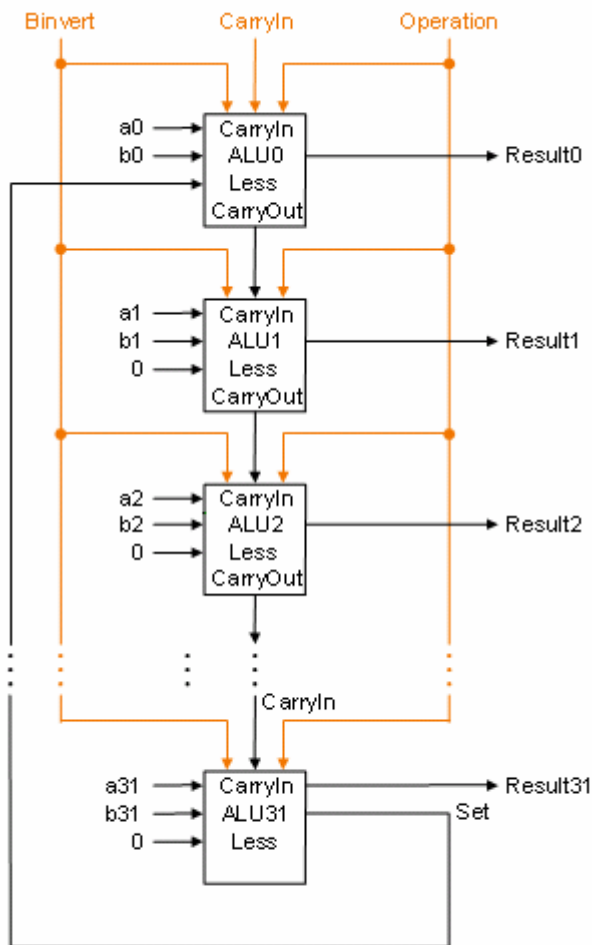
- a. bne
- b. jr
- c. lui

3. [5 points each] For each of the problems below, modify the 32-bit ripple-carry ALU developed in class as indicated. Use only inverters, AND gates, OR gates, and multiplexers. In each case, describe any new or modified control signals. Also, assuming that the ALU is currently on the critical path for your design, determine whether or not your modifications would extend the clock cycle time.
- a. Modify the ALU to support the MIPS `xor` instruction.
 - b. Modify the ALU so that it detects overflow for both addition and subtraction (i.e. so that it has a new 1-bit output called `Overflow` which is asserted iff overflow occurs). Read pages 170-172 of your textbook and Figure 3.3 for more information.
 - c. Modify the ALU so that it implements `slt` correctly even when overflow occurs. Assume that you have a combinational logic unit that detects overflow, as you are required to design for the previous problem.

The figures for a 1-bit ALU and 32-bit ALU are available on the next page.



1-bit ALU



32-bit ALU