Rose-Hulman Institute of Technology
Computer Science and Software Engineering
Profs. Archana Chidanandan and Larry Merkle

Homework 3
Register Transfer Language
Max Points: 45 points

Directions

This assignment is due Tuesday, October 10 for all three sections. Submit your solutions on a separate sheet of paper.

Learning Objectives

In the process of completing this homework assignment, students will develop their abilities to

- Describe the implementation of machine language instructions using Register Transfer Language.
- Identify the components required to implement machine language instructions, including their input, output, and control signals, as well as their high-level behavior.
- Determine how to handle exceptions, including interrupts.

Problems

1. [15 pts] Consider the MIPS instructions `jr`, `sll`, and `lui`.

   a. Write a multicycle RTL description of an implementation of each instruction that uses as few cycles as possible without extending the clock cycle of your design.

   b. Identify any "new components" required to implement each of the instructions. Describe their input, output, and control signals, as well as their high-level behavior. In this context, "new components" means components that are not shown in Figure 5.28 of Patterson & Hennessy.

2. [10 pts] Consider the MIPS instructions `mfc0`, and `mtc0`. Write a multicycle RTL description of an implementation of each instruction that uses as few cycles as possible without extending the clock cycle of your design. You are NOT required to identify the new components. *Hint:* Page A71 (on the CD) of Hennessey and Patterson, has descriptions for these two instructions.

3. [10 pts] Write a multicycle RTL description of an "undefined" instruction that uses as few cycles as possible without extending the clock cycle of your design. *Hint:* Save PC-4 in EPC, modify the PC, and update the Status Register. Read through pages 340-343 and pages A33-A35 (on the CD) of Patterson and Hennessy for more information (keeping in mind that for this exercise you are NOT concerned with the datapath or control system).

4. Consider the (fictitious) MIPS instruction `addmem` described below.

   ```
   addmem rd, rs, rt
   ```

   The instruction reads the values from the memory locations indexed by the contents of registers `rs` and `rt`, adds the values, and stores the result in the memory location indexed by the contents of register `rd`.

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a. [5 pts] Write a multicycle RTL description of an implementation of the addmem instruction that uses as few cycles as possible without extending the clock cycle of your design.

b. [5 pts] Write a single cycle RTL description of an implementation of the addmem instruction.