

RTL descriptions for MIPS instructions

Clock cycle	R-Type	sw	lw	beq	j
1	IR = Mem[PC] PC = PC + 4				
2	A = Reg[IR[25:21]] B = Reg[IR[20:16]] ALUOut = PC + (SE(IR[15:0]) << 2) If(IR[31:26] == xxxxxx) and if(IR[5:0]==xxxxx) then				
3	ALUOut = A op B	ALUOut = A + SE(IR[15:0])	If(A-B= =0) then PC = ALUOut	PC = PC[31:28] IR[25:0] 00	
4	Reg[IR[15:11]] = ALUOut	Mem[ALUOut] = B	MDR = Memory[ALUOut]		
5			Reg[IR[20:16]] = MDR		