

## Syllabus<sup>1</sup>

Week starting	Day	Topics	Reading (Sections)	Due
11/29	T	Course overview/Project Overview		
	W	Intro. To MIPS, SPIM*	2.3,2.5	
	R	Conditional statements*	2.6	Teams, Proposed meeting times <sup>2</sup>
12/06	T	Procedures*	2.7	
	W	Addressing modes*	2.9	
	R	Representing instructions*	2.4	
12/13	T	Exceptions		
	W	Computer arithmetic/Xilinx installation	3.3	
	R	Xilinx exercise		Assembly Language and Machine Language specifications (M1)
<b>Winter break</b>				
01/03	T	Group Meetings and Project Time		
	W	Register Transfer Language	5.5	
	R	Exam 1		
01/10	T	Exceptions/ Xilinx exercise		
	W	Single cycle datapath implementation	5.3-4	
	R	Multi-cycle datapath implementation	5.5	RTL Specifications (M2)
01/17	T	ALU Design/ Xilinx Exercise	3.3	
	W	Xilinx Exercise		
	R	Group Meetings and Project Time		
01/24	T	Control design (FSM)/ Xilinx Exercise	5.5	Datapath Design and Component Specification. (M3)
	W	Control design (Micro-programming)/Xilinx Exercise	5.53-54	
	R	Group Meetings and Project Time		
01/31	T	Xilinx Exercise		
	W	Performance	Ch. 4	
	R	Group meetings and project time		Control unit design and components implementation (M4)
02/07	T	Floating Point	3.30-31,48	
	W	Recursion and stacks	2.7	
	R	Group meetings and project time		Component Integration and Datapath Testing (M5)
02/14	T	Exam 2		
	W	Group meetings and project time		
	R	Group meetings and project time		Final Xilinx model
02/21		<b>Finals week (Project Presentations)</b>		

<sup>1</sup> This is a tentative schedule. It may be changed at the discretion of the instructor.

<sup>2</sup> See the CSSE 232 (03-04 Winter) Term Project Requirements document for details about term project turn-ins.