Rose-Hulman Institute of Technology
Computer Science and Software Engineering
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Homework 2
(Exceptions, Register Transfer Language and Datapaths)
Maximum points: 55 points + 15 extra credit points

Directions

This assignment is due Tuesday, Oct. 12th for Sections 1, 2 and 3. Submit your solutions on a separate sheet of paper.

Learning Objectives

In the process of completing this homework assignment, students will develop their abilities to

- Describe the implementation of machine language instructions using Register Transfer Language.
- Identify the components required to implement machine language instructions, including their input, output, and control signals, as well as their high-level behavior.
- Design datapaths to support machine language instruction sets by specifying the interconnections between components and the behavior of the associated control units.
- Determine how to handle exceptions, including interrupts.

Problems

1. Figure 5.28 of Patterson & Hennessy, shows a complete datapath for a multicycle implementation of most R-Type MIPS assembly language instructions, as well as `lw`, `sw`, `beq`, and `j`. For this question, you are required to modify the datapath to include the multicycle implementation of the `bne` instruction. Specifically, you must:

   a. [5 points] Write a multicycle RTL description of an implementation of the `bne` instruction that uses as few cycles as possible without extending the clock cycle of your design.

   b. [5 points] List all new and modified components required for the implementation of the `bne` instruction. Also, list the input, output, and control signals for each of those components. Indicate the number of bits in each signal.

   c. [5 points] Add any necessary datapath components and control signals to the multicycle datapath. A pdf version of Figure 5.28 is available on the class website(Homework).

2. [15 points] Repeat Steps 1a, 1b and 1c for the `mfc0` and `mtc0` MIPS instructions (combine the component lists and the datapath modifications). *Hint:* Page A71 (on the CD) of Hennessey and Patterson, has a description for these two instructions.

3. [10 points] Repeat Steps 1a and 1b for an "undefined" instruction in MIPS. Figure 5.39 in your textbook, shows the modifications required for the datapath. *Hint:* Save PC-4 in EPC, modify the PC, and update the Status Register. Read through pages

340-343 and pages A33-A35 (on the CD) of Patterson and Hennessy for more information.

4. Figure 5.24 of Patterson & Hennessy, shows a complete datapath for a single-cycle implementation of most R-Type MIPS assembly language instructions, as well as `lw`, `sw`, `beq`, and `j`. For this question, you are required to modify the datapath to include the single cycle implementation of the `bne` instruction.

   a. [5 points] Write a single-cycle RTL description of an implementation of the `bne` instruction.

   b. [5 points] List all new and modified components required for the implementation of the `bne` instruction. Also, list the input, output, and control signals for each of those components. Indicate the number of bits in each signal.

   c. [5 points] Add any necessary datapath components and control signals to the single-cycle datapath. A pdf version of Figure 5.24 is available on the class website(Homework).

5. [15 points for Extra Credit] Consider a variant of the `lw` instruction `lwr`. The `lwr` instruction sums two registers to obtain the address of the data to be loaded and uses the R-format.

   ```
   lwr rd, rs, rt
   ```

   The instruction must read a value from memory and store it in register `rd`. The address, of the value in memory, is determined by adding the contents of registers `rs` and `rt`.

   Repeat Steps 1a, 1b and 1c for the `lwr` instruction for a multi-cycle datapath.