Rose-Hulman Institute of Technology
Computer Science and Software Engineering
Prof. Archana Chidanandan

Homework 6
Computer Arithmetic and Performance
Maximum points: 60

Directions
This assignment is due Tuesday, 10th February 2004 by 5:00 PM for Sections 1 and 2.

Learning Objectives
In the process of completing this homework assignment, students will develop their abilities to
- Design digital logic circuits for computer arithmetic.
- Predict the qualitative effect on clock cycle time of modifications to the design of digital logic circuits.
- Determine the absolute and relative performance of implementations of instruction set architectures.

General Instructions
1. Submit your solutions on a separate sheet of paper.
2. Remember that the figures in the book are available in electronic form on the book's website and on the class website(Resources).
3. Use only inverters, AND gates, OR gates, and multiplexers for problems 1 to 5.

Problems
1) [5 points] Modify the 32-bit ripple-carry ALU developed in class to support the MIPS XOR instruction. Describe any new or modified control signals.

2) [5 points] Modify the 32-bit ripple-carry ALU developed in class so that it detects overflow for both addition and subtraction (i.e. so that it has a new 1-bit output called Overflow which is asserted iff overflow occurs). *Hint:* There are four cases to consider. One of them is the case in which both inputs are positive and the sum appears to be negative. Look up pages 221 and 222(Figure 4.4) of Hennessy and Patterson for more information.

3) [5 points] Assume that you have a combinational logic unit that detects overflow, as you are required to design for Problem 2. Modify the 32-bit ripple-carry ALU developed in class so that it implements SLT correctly even when overflow occurs.

4) [5 points] Your design team makes frequent use of the MIPS pseudoinstruction ABS, which determines the absolute value of a value in a source register. You are considering modifying the processor to make it an actual instruction. Show the necessary modifications to the 32-bit ripple-carry ALU developed in class to support the new instruction. Describe any new or modified control signals.

5) [5 points] Assume that the ALU is currently on the critical path for your design. Determine whether or not each of your modifications would extend the clock cycle time. State any additional assumptions.

6) [5 points] Problem 2.14 from Patterson and Hennessy.

7) In this problem, you will analyze the performance of two implementations of the MULDER instruction set architecture.

   a. [5 points] For the FOX implementation, the clock rate is 1 GHz, and instructions fall into two categories. Category X instructions require 4 cycles to execute, while category Y instructions require 5 cycles. If the File program executes 1.27×10^{11} category X instructions and 1.01×10^{11} category Y instructions, how long will it take to execute? Express your answer in seconds.

   b. [5 points] The SPOOKY implementation is identical to the FOX implementation, except that the clock rate is 1.2 GHz and category Y instructions require 6 cycles. How long will the File program take to execute on this implementation?

   c. [5 points] The AGENT implementation is identical to the FOX implementation, except that it includes a category Z instruction that requires 8 cycles to execute and does the same thing as a common combination consisting of one category X instruction and one category Y instruction. This combination accounts for 10% of the category X instructions used by the File program on the FOX implementation. How long will the File program take to execute on the AGENT implementation?

   d. [5 points] Between the FOX and SPOOKY implementations, which is faster for the File program, and by how much?

8) [10 points] Problem 2.13 from Patterson and Hennessy.