

General Information:

Registers:

- Four general purpose 16-bit registers (\$A-\$D)
- One special purpose 8-bit Data Segment register (DS)
- One special purpose 16-bit Stack Pointer register (SP)
- One special purpose 4-bit Conditional Flag register (Flags)
- One special purpose 16-bit Display Register (DR)

I/O:

- Memory-mapped I/O via the 0xFF Data Segment.

Interrupts:

- Supports up to four prioritized interrupts.
- Lower number interrupt takes priority over higher.
- Interrupt routines should disable interrupts on entrance and re-enable interrupts on exit, to prevent further interruption.

Condition Flags:

- Flags = {EQ, GT, OV, LT} and the negated {NEQ, NGT, NOV, NLT}
- EQ = Equal, GT = Greater Than, OV = Overflow, LT = Less Than
- Only one flag at a time can be used as a conditional.
- Only CP/I set the condition flags.
- Overflow is set by any mathematical instruction.

Special Data Movement:

STDSI VAL

Change the data segment to VAL

STDS RS

Change the data segment to RS

LDDS RD

Load the current data segment into RD

STSP RS

Change stack pointer to RS

LDSP RD

Load the current stack pointer into RD

STFI VAL

Change the flag register to LSB of VAL

STF RS

Change the flag register to the LSB of RS

LDF RD

Load the current flag values into the LSB of RD

STDR RS

Change the display register to RS

LDDR RD

Load the display register into RD

Data Movement:

LD RD, (ADDR)

Load data from an immediate memory address DS:ADDR into RD

ST (ADDR), RS

Store data from RS to an immediate memory address DS:ADDR

LDRI RD, (RS)

Load data from memory specified by RS into RD

STRI (RD), RS

Store data from RS into the memory address specified by RD

LDR RD, RS

Load value from RS into RD

LDIU RD, VAL

Load an immediate value VAL into upper-half of RD

LDIL RD, VAL

Load an immediate value VAL into lower-half of RD

PUSH RD

Load value RD to (SP), decrement SP

POP RD

Load value from (SP) to RD, increment SP

Arithmetic:

ADD RD, RS

Add RS to RD

ADDI RD, VAL

Add VAL to RD

SUB RD, RS

Subtract RS from RD

SUBI RD, VAL

Subtract VAL from RD

NEG RD

2's-complement of RD

Logical:

OR RD, RS

Bitwise-OR RD against RS

ORI RD, VAL

Bitwise-OR RD against VAL

AND RD, RS

Bitwise-AND RD against RS

ANDI RD, VAL

Bitwise-AND RD against VAL

SLL RD, RS

Logical shift left RD by RS bits

SLLI RD, VAL

Logical shift left RD by VAL bits

SLR RD, RS

Logical shift right RD by RS bits

SLRI RD, VAL

Logical shift right RD by VAL bits

Program Control:

JP RS

Unconditional jump to the address specified by RS

JP ADDR

Unconditional jump to an immediate address ADDR; sets PC to ADDR

JP C, ADDR

Jump, when the condition-satisfied flag is set, to an immediate address ADDR; sets PC to ADDR

JP NC, ADDR

Jump, when the condition-satisfied flag is unset, to an immediate address ADDR; sets PC to ADDR

CALL RS

Unconditional call to the address specified by RS; sets (SP) to the PC of the following instruction, increments SP, sets PC to the value in RS

CALL ADDR

Unconditional jump to an immediate address ADDR; sets (SP) to the PC of the following instruction, increments SP, sets PC to ADDR

CALL C, ADDR

Jump, when the condition-satisfied flag is set, to an immediate address ADDR; sets (SP) to the PC of the following instruction, increments SP, sets PC to ADDR

CALL NC, ADDR

Jump, when the condition-satisfied flag is unset, to an immediate address ADDR; sets (SP) to the PC of the following instruction, increments SP, sets PC to ADDR

RET

Decrement SP, jump to (SP)

RET C

When the condition-satisfied flag is set, decrement SP, jump to (SP)

RET NC

When the condition-satisfied flag is unset, decrement SP, jump to (SP)

Comparisons:

CP RD, RS

Sets the condition flags based on RD vs. RS. (Flags: Equal, Greater Than, Overflow, Less Than)

CPI RD, VAL

Sets the condition flags based on RD vs. VAL. (Flags: Equal, Greater Than, Overflow, Less Than)

Interrupts:

SETII INT#, ADDR

Set interrupt INT# to DS:ADDR

SETI INT#, RS

Set interrupt INT# to RS

GETI RD, INT#

Get the address of INT# into RD

Basic Instruction Format:

Type	Opcode	(Varies)
2-bits	4-bits	10-bits

Instruction Types:

- [S]ingle Register

Type	Opcode	Register (Source/Destination)	Unused
00	4-bits	2-bits	8-bits

- [B]ranch

Type	Opcode	Condition	Immediate
01	4-bits	2-bits	8-bits

Type	Opcode	Condition	Register Source	Unused
01	4-bits	2-bits	2-bits	6-bits

- [P]aired Registers

Type	Opcode	Register Destination	Register Source	Unused
10	4-bits	2-bits	2-bits	6-bits

- [I]mmediate

Type	Opcode	Register (Source/Destination)	Immediate
11	4-bits	2-bits	8-bits

Register Conversions:

\$A = 00
 \$B = 01
 \$C = 10
 \$D = 11

Interrupt Conversions:

INT0 = 00
 INT1 = 01
 INT2 = 10
 INT3 = 11

Condition Codes:

EQ = 00
 GT = 01

OV = 10

LT = 11

Special Data Movement:

STDSI VAL: I-Type

11	0000	XX	VAL
----	------	----	-----

STDS RS: S-Type

00	0011	RS	XXXXXXXX
----	------	----	----------

LDDS RD: S-Type

00	0011	RD	XXXXXXXX
----	------	----	----------

STSP RS: S-Type

00	0101	RS	XXXXXXXX
----	------	----	----------

LDSP RD: S-Type

00	0110	RD	XXXXXXXX
----	------	----	----------

STFI VAL: I-Type

11	0001	XX	VAL
----	------	----	-----

STF RS: S-Type

00	1001	RS	XXXXXXXX
----	------	----	----------

LDF RD: S-Type

00	1010	RD	XXXXXXXX
----	------	----	----------

STDR RS: S-Type

00	0111	RS	XXXXXXXX
----	------	----	----------

LDDR RD: S-Type

00	1000	RD	XXXXXXXX
----	------	----	----------

Data Movement:

LD RD, (ADDR): I-Type

11	0010	RD	LSB[ADDR]
----	------	----	-----------

ST (ADDR), RS: I-Type

11	0011	RS	LSB[ADDR]
----	------	----	-----------

LDRI RD, (RS): P-Type

10	0000	RD	RS	XXXXXX
----	------	----	----	--------

STRI (RD), RS: P-Type

10	0001	RD	RS	XXXXXX
----	------	----	----	--------

LDR RD, RS: P-Type

10	0010	RD	RS	XXXXXX
----	------	----	----	--------

LDIU RD, VAL: I-Type

11	0100	RD	VAL
----	------	----	-----

LDIL RD, VAL: I-Type

11	0101	RD	VAL
----	------	----	-----

PUSH RD: S-Type

00	1011	RD	XXXXXXXX
----	------	----	----------

POP RD: S-Type

00	1100	RS	XXXXXXXX
----	------	----	----------

Arithmetic:

ADD RD, RS: P-Type

10	0011	RD	RS	XXXXXX
----	------	----	----	--------

ADDI RD, VAL: I-Type

11	0110	RD	VAL
----	------	----	-----

SUB RD, RS: P-Type

10	0100	RD	RS	XXXXXX
----	------	----	----	--------

SUBI RD, VAL: I-Type

11	0111	RD	VAL
----	------	----	-----

NEG RD: S-Type

00	1101	RD	XXXXXXXX
----	------	----	----------

Logical:

OR RD, RS: P-Type

10	0101	RD	RS	XXXXXX
----	------	----	----	--------

ORI RD, VAL: I-Type

11	1000	RD	VAL
----	------	----	-----

AND RD, RS: P-Type

10	0110	RD	RS	XXXXXX
----	------	----	----	--------

ANDI RD, VAL: I-Type

11	1001	RD	VAL
----	------	----	-----

SLL RD, RS: P-Type

10	0101	RD	RS	XXXXXX
----	------	----	----	--------

SLLI RD, VAL: I-Type

11	1010	RD	VAL
----	------	----	-----

SLR RD, RS: P-Type

10	0110	RD	RS	XXXXXX
----	------	----	----	--------

SLRI RD, VAL: I-Type

11	1011	RD	VAL
----	------	----	-----

Program Control:

JP RS: B-Type

01	0000	XX	RS	XXXXXX
----	------	----	----	--------

JP ADDR: B-Type

01	0001	XX	LSB[ADDR]
----	------	----	-----------

JP C, ADDR: B-Type

01	0010	C	LSB[ADDR]
----	------	---	-----------

JP NC, ADDR: B-Type

01	0011	C	LSB[ADDR]
----	------	---	-----------

CALL RS: B-Type

01	0100	XX	RS	XXXXXX
----	------	----	----	--------

CALL ADDR: B-Type

01	0101	XX	LSB[ADDR]
----	------	----	-----------

CALL C, ADDR: B-Type

01	0110	C	LSB[ADDR]
----	------	---	-----------

CALL NC, ADDR: B-Type

01	0111	C	LSB[ADDR]
----	------	---	-----------

RET: B-Type

01	1000	XXXXXXXXXX
----	------	------------

RET C: B-Type

01	1001	C	XXXXXXXXXX
----	------	---	------------

RET NC: B-Type

01	1010	C	XXXXXXXXXX
----	------	---	------------

Comparisons:

CP RD, RS: P-Type

10	0111	RD	RS	XXXXXX
----	------	----	----	--------

CPI RD, VAL: I-Type

11	1100	RD	VAL
----	------	----	-----

Interrupts:

SETII INT#, ADDR: I-Type

11	1101	INT#	LSB[ADDR]
----	------	------	-----------

SETI INT#, RS: P-Type

10	1000	INT#	RS	XXXXXX
----	------	------	----	--------

GETI RD, INT#: P-Type

10	1000	RD	INT#	XXXXXX
----	------	----	------	--------