Rose-Hulman Institute of Technology
Computer Science and Software Engineering
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Homework 3
(RTL, Datapath and Exception Handling)

This assignment is due Tuesday, October 7, 2003 for Sections 1, 2 and 3. Submit your solutions on a separate sheet of paper.

Learning Objectives

In the process of completing this homework assignment, students will develop their abilities to

- Describe the implementation of machine language instructions using Register Transfer Language.
- Identify the components required to implement machine language instructions, including their input, output, and control signals, as well as their high-level behavior.
- Design datapaths to support machine language instruction sets by specifying the interconnections between components and the behavior of the associated control units.
- Determine how to handle exceptions, including interrupts.

Problems

1. Figure 5.33 of Patterson & Hennessy, shows a complete datapath for a multicycle implementation of most R-Type MIPS assembly language instructions, as well as `lw`, `sw`, `beq`, and `j`. For this question, you are required to modify the datapath to include the multicycle implementation of the `lui` instruction. Specifically, you must:

    a. [5 points] Write a multicycle RTL description of an implementation of the `lui` instruction that uses as few cycles as possible without extending the clock cycle of your design.

    b. [5 points] List all new and modified components required for the implementation of the `lui` instruction. Also, list the input, output, and control signals for each of those components. Indicate the number of bits in each signal.

    c. [5 points] Add any necessary datapaths and control signals to the multicycle datapath. You can photocopy existing figures or download figures from www.mkp.com/cod2e.htm to make it easier to show your modifications.

2. [15 points] Repeat Steps 1a, 1b and 1c for the `mfc0` and `mtc0` MIPS instructions (combine the component lists and the datapath modifications).

3. [15 points] Repeats Steps 1a, 1b and 1c for an "undefined" instruction in MIPS. *Hint:* Save PC-4 in EPC, modify the PC, and update the Status Register. Read through pages 410-413 of Patterson and Hennessy for more information.

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4. [5 points] In question 1 of this assignment, you wrote the RTL description for the lui instruction. For question 4, you must modify the RTL description for lui, to handle an interrupt i.e. an unexpected event that occurs outside the processor, and causes a change in the flow of execution of the program. *Note:* You do not need to list the new and modified components, nor do you need to show the modified datapath.