Rose-Hulman Institute of Technology
Computer Science and Software Engineering
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Homework 2
(Assembly and Machine Languages)

This assignment is due Monday, September 29, 2003 for Sections 1 and 3 and on Tuesday, September 30, 2003 for Section 2. Submit your solutions on a separate sheet of paper.

Learning Objectives

In the process of completing this homework assignment, students will develop their abilities to

- Translate assembly language instructions into machine language.
- Interpret a sequence of bits and determine what it represents.
- Determine addressing in branches and jumps.
- Interpret instruction formats and fields.

Problems

1. [5 pts] List the machine language fields and their binary values for these MIPS instructions:

```
add     $t0, $s0, $s1
addi    $t0, $s0, 150
lw      $t0, 150($s0)
slt     $t0, $s0, $s1
jr      $t0
```

2. [4 pts] Assume that the MIPS instruction `beq $t0, $s0, Label` is located at address `0x0400 1234`, and that `Label` is located at address `0x0400 5678`. What will the binary value of the address field be? *Hint*: remember that the offset is relative to the instruction following the branch, and that all branch targets must be word aligned.

3. [4 pts] Assume that the MIPS instruction `j Label` is located at address `0x0400 1234`, and that `Label` is located at address `0x0400 5678`. What will the binary value of the target address field be? *Hint*: remember that all branch targets must be word aligned.

4. [2 pts] What sequence of two MIPS instructions starting at address `0x0400 1234` could be used to branch to address `0x4400 5678`?

5. [4 pts] A computer has a 32-bit word length, and all the instructions are one word in length. Every instruction has a two bit field which specifies the instruction type. The number of registers (the register file) in the architecture of the computer is 64.
    a. For a format that has an opcode field to determine the function of the instruction and three register fields, what is the maximum number of opcodes possible?
    b. For a format with two register fields, one immediate/address field, and a maximum of 256 opcodes, what is the maximum number of bits available for the immediate/address field?

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6. [6 pts] Bits have no inherent meaning. However, given the rules to interpret them, a sequence of bits can represent different values and have meaning. Given the following 32-bit pattern:

   1000 1101 0010 1001 0000 0000 0000 0000

   what does it represent, assuming that it is

   a. a two's complement integer?
   b. an unsigned integer?
   c. a MIPS instruction?