Rose-Hulman Institute of Technology
Computer Science and Software Engineering
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Term Project Milestone 3 Evaluation (Datapath and Control Specifications)

Evaluation Criteria Categories	Specific Criteria	Comments	Score
Consistency with higher level specifications	❑ State elements that are assigned or referenced in Register Transfer Language (RTL) statements appear in datapath ❑ Operations that are required to implement RTL statements have corresponding components ❑ Inputs, outputs, and control signals of components in datapath are consistent with RTL specification ❑ Connections between components in datapath are consistent with RTL specification ❑ The control signals specified for each state (or microstep) produce the register transfers specified in the corresponding cycle of the RTL description	The datapath contains appropriate state elements. The datapath appears to correctly implement RTL. RTL specification for goeq differs from FSM; uses ALU twice in one cycle. Connections appear reasonable. Control signals implement RTL.	3/3
Self-consistency	❑ Input signals that have multiple sources have associated multiplexers ❑ Multiplexers have appropriately sized control signals ❑ Datapath includes one or more control units that generate the necessary control signals and have the appropriate input signals ❑ The value of each control signal is defined for every state (or microstep)	Multiplexors are used to connect multiple inputs. Bus signal sizes not noted on datapath. Control unit controls datapath. Control signals are reasonably defined—though you should not missing signals are not asserted.	2/3
Demonstration of design principles 1. Simplicity favors regularity 2. Smaller is faster 3. Good design demands good compromises 4. Make the common case fast	❑ Components are kept as simple as possible ❑ Similar components used by multiple instructions or in multiple cycles are combined where possible ❑ Tradeoffs between the preceding criteria favor the common case, not the special case ❑ Regularity in the machine language format is exploited by using combinational logic where feasible ❑ Identical states (or microsteps) are combined	Why is it necessary to read three registers in a cycle? Can you use instruction regularity to eliminate one? Components are reused appropriately. Fifth cycles of some R-type instructions are identical. Should probably be combined into writeback cycle. Variable shifts will cause a long signal path—probably want to buffer the output, adding an extra cycle.	2/3

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Documentation (see below) ❑ Organization ❑ Completeness ❑ Conciseness ❑ Grammar and style	❑ Datapath diagram ❑ Clear English specifications o Effects of control signals ❑ Datapath tests ❑ State transition diagram or microprogram specifying the finite state machine ❑ Truth tables or Boolean equations specifying any combinational units ❑ Clear English specifications as necessary ❑ Control unit tests	Memo is ok; needs to assess progress on milestone. Design Process Documentation is acceptable, would benefit from more rationale behind decisions. Design Documentation is detailed, shows significant effort. It is slightly long, however, and the datapath is almost small enough to be difficult to read. Still, much improved from last milestone. Website shows effort, links to relevant files.	15/16

Required Documents

- Memo
  - Objective assessment of design and status
- Design Documentation
  - Demonstration of conceptual understanding
  - Highlights interesting features
- Design Process Journal
  - Alternatives considered
  - Tradeoffs
  - Decisions
- Website