ECE250 Lab Project #7

BJT Common-Collector (Emitter-Follower) Amplifier

Dept. of Electrical and Computer Engineering (KEH)
Rose-Hulman Institute of Technology (last updated on 5/1/2009)

Lab Team Members: _____   _____

Date Performed: _____   **Lab Station:** _____

PRELAB (This prelab activity __must be completed before__ coming to lab!)
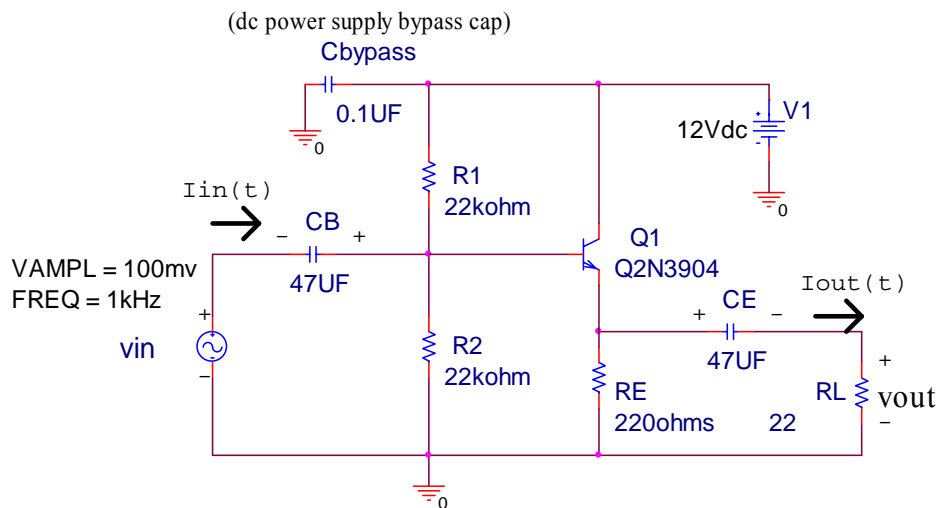

Figure 1: Common Collector (CC) NPN BJT Amplifier

Assuming that the transistor in Figure 1 has the following parameters: **β_F = 200, n = 1.3, and Vbeon = 0.7 V,** create a Maple Worksheet that allows these parameters to be defined at the top of the worksheet and calculates the following information:

- Q-point: Icq and Vceq
- Output resistance "Rout" looking back from the load resistor (RL) terminals (do not include RL in this calculation.)
- Input resistance "Rin" looking in from the amplifier input terminals, first with RL removed, and then with RL present.
- The unloaded small-signal voltage gain: Avo = vout/vin with RL removed.
- The loaded small-signal voltage gain: Av = vout/vin with RL present.
- The maximum symmetrical output voltage swing (volts, peak-to-peak) with the load resistor (RL = 22 Ω) in place.

__Clearly box in the results and pencil in appropriate units on your Maple Worksheet.__
Your worksheet __MUST__ come up with the following "hand predictions":

Icq = 19.2 mA and Vceq = 7.76 V	Rout = 1.74 ohms
Rin_RL_removed = 8.82 kohms	Rin_RL_present = 3.13 kohms
Avo = 0.992	Av = 0.920
Maximum symmetrical output swing = 0.77V peak-peak	

LAB:

1. Measure the β of your transistor:

    Obtain a 2N3904 NPN BJT from the instrument room. The pin-
    outs for the epoxy-packaged version of this BJT is shown in Fig.
    2. Measure the value of β_F for your transistor at or near the
    desired operating point (use the ICQ & VCEQ from your prelab)
    using the curve tracer.

    2N3904 (NPN) β_F = _____
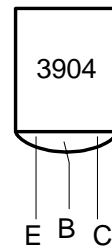
Flat Side Front

3904

E B C

Figure 2: Pinout of
2N3904 & 2N3906

2. Update your prelab calculations:

    Change the β value from the prelab spreadsheet to the value that corresponds to your 2N3904 BJT,
    and enter the results in the blanks below (you may continue to assume Vbeon = 0.7 V and n = 1.5.
    Attach the modified (using your measured value of β_F) prelab spreadsheet as **Attachment A**.

    Predicted Results with updated β_F:

    Q-point: Icq = _____ mA,   Vceq = _____ V

    Rin (with RL in place) = _____ kilohms   Rout = _____ ohms

    Av = _____

    Maximum symmetrical output swing = _____ V peak-peak

3. Build the circuit:

    Now build the circuit shown in Figure 1. Be sure to include the dc power bypass capacitor
    (Cbypass), whose value is not critical, but is generally between 0.1 uF and 0.01 uF). This capacitor
    should be placed directly across the dc power distribution bus (between Vcc and ground), as close as
    possible to the emitter-follower BJT collector terminal and where its emitter resistor is connected to
    the ground bus. Its purpose is to filter out (act as a short circuit for) any ac noise that is present on
    the dc power distribution bus. Such noise might be generated by the sudden current demands made
    by the amplifier circuit itself as it operates. Without this capacitor, it is possible that this amplifier
    circuit may oscillate rather than amplify! This is because, upon powering up the circuit, a sudden
    current demand is made from the dc power bus as the coupling capacitors charge to their equilibrium
    values. However, if there is no "local reservoir of charge" (a capacitor) located near the BJT to
    supply this sudden current demand, a sudden voltage drop could occur across the parasitic
    (unwanted) inductance of the dc power bus wiring, which could cause a second turn-on transient to
    occur a little later, which in turn could cause a second sudden voltage drop on the dc power bus, etc.
    This vicious cycle might result in an undesired oscillation that can continue indefinitely.

Another possible oscillation mode that might develop on your breadboard is due to capacitive coupling of the output back to the input. Even though this circuit exhibits less than unity voltage gain between base and emitter, the presence of parasitic wire inductance in the collector circuit might permit this circuit to exhibit a high voltage gain between base and collector at very high radio (RF) frequencies. Whether such RF oscillation will occur depends upon your breadboard layout, and how short your wires are, etc_. **_In order to "nip" this possible RF oscillation problem "in the bud", please stabilize your circuit by connecting a 0.01 µF capacitor, with its leads cut short to minimize parasitic lead inductance, directly between the collector and emitter terminals of the BJT to ground._** This will "short out" any high frequency signal oscillations, while still passing the desired audio frequencies. Note that the impedance of a 0.01 µF capacitor at the signal frequency (1 kHz) has a magnitude of $1/(2\pi fC) = 16$ kΩ, so this capacitor should not significantly interfere with circuit operation at the signal frequency.

4. Measure the Bias Point:

   Use your DVM to measure the Q-point (VCE_Q and I_{CQ}). Measure I_{CQ} indirectly, by measuring the dc voltage across emitter resistor R_E, or V_{EQ}. Your Q-point should not be off by more than 25% from your predictions!

            Icq = _____ mA   % Err = _____

            Vceq = _____ V   %Err = _____

5. Measure the Small Signal Gain:

   Set Vin(t) for a 200 mV peak-to-peak sine wave at 1 kHz, and measure the (loaded) AC voltage gain, Av = vout/vin.

            Av = _____   %Err = _____

   Capture an oscilloscope picture showing both the input and output waveforms along with measured valued of the input frequency and both the input and output peak to peak magnitudes. Include this picture as **Attachment B.**

6. Measure the Small Signal Input Resistance:

   Next, experimentally determine the input resistance "Rin" by temporarily connecting a "current-sensing" resistor Rx =10 kΩ between the generator (+) terminal and the input coupling capacitor CB. Use your oscilloscope to measure the peak-to-peak amplitudes of the sinusoidal voltages on each side of this resistor with respect to ground. Let us call the peak-to-peak voltage amplitude measured (with respect to ground) on the left side of this resistor *Vgen*, and the peak-to-peak voltage amplitude measured (with respect to ground) on the right side of this resistor *Vcb*. Then the difference between these two peak-to-peak voltage amplitude readings *Vgen – Vcb* must be the peak-to-peak voltage amplitude developed across the current-sensing resistor Rx. Dividing this by the value of Rx gives the input current amplitude, and therefore dividing this result into *Vcb* yields the input resistance, Rin, of the amplifier. Thus

   $$Rin = \frac{Vcb}{Ix} = \frac{Vcb}{(Vgen - Vcb)/Rx}$$

Now compare your observed Rin value with the hand-calculated value you obtained previously (it should be within 20%).

        Vgen = _____ mV

        Vcb = _____ mV

        Rin = _____ kΩ   %Err = _____

Now ***remove Rx***, restoring the circuit to its original state, as shown in Fig. 1.

7. Measure the Small Signal Output Resistance:

To measure the output resistance "Rout" of the amplifier, measure the peak-to-peak value of Vout across the load resistor RL = 22 ohms; let us call this voltage *Vout_loaded*. Next, remove the load resistor RL, and note the (very slightly increased) peak-to-peak value of Vout; let us call this value *Vout_unloaded*. Now the amplifier is said to have an "unloaded output", and the value of Vout corresponds to the (internal) Thevenin equivalent voltage source "Vth" that is effectively in series with Rout. Thus Rout can be found by solving the following voltage divider equation that holds when RL is present:

$$Vout\_loaded = Vout\_unloaded * RL / (RL + Rout)$$

Now you can solve this equation for Rout and compare your observed value with the hand calculated value obtained previously. (Your predicted value should be on the order of several ohms.) You do not need to calculate the percent error for Rout because the model that we used for the calculations neglected the resistance between the terminals and the internal device which can be on the order of an ohm.

        Vout_loaded = _____ V

        Vout_unloaded = _____ V

        Rout = _____ Ω   (Should be ≈ 2 Ω)

Make sure the 22Ω resistor is put back into your circuit to restore it to its original state.

8. Measure the Maximum Output Swing:

Experimentally measure the maximum symmetrical output voltage swing exhibited by your circuit (across the 22 Ω load resistor) by turning up the function generator voltage amplitude until the output waveform begins to flatten on one end or the other. Capture an oscilloscope picture showing both the input and output waveforms under the conditions when the output is beginning to distort. Make sure this picture shows the frequency of the input along with the peak to peak magnitude of both the input and output. Include this picture in your lab report as **Attachment C**.

Now reduce the input amplitude just below the point where the output waveform begins to flatten. The peak-to-peak value of this waveform corresponds to the observed "*maximum symmetrical output voltage swing*". Make a note of the peak to peak output voltage under these conditions in the table below.

Maximum symmetrical output swing = _____ V peak-peak

%Err = _____

Figure 3. Complete Complementary Symmetry Audio Amplifier
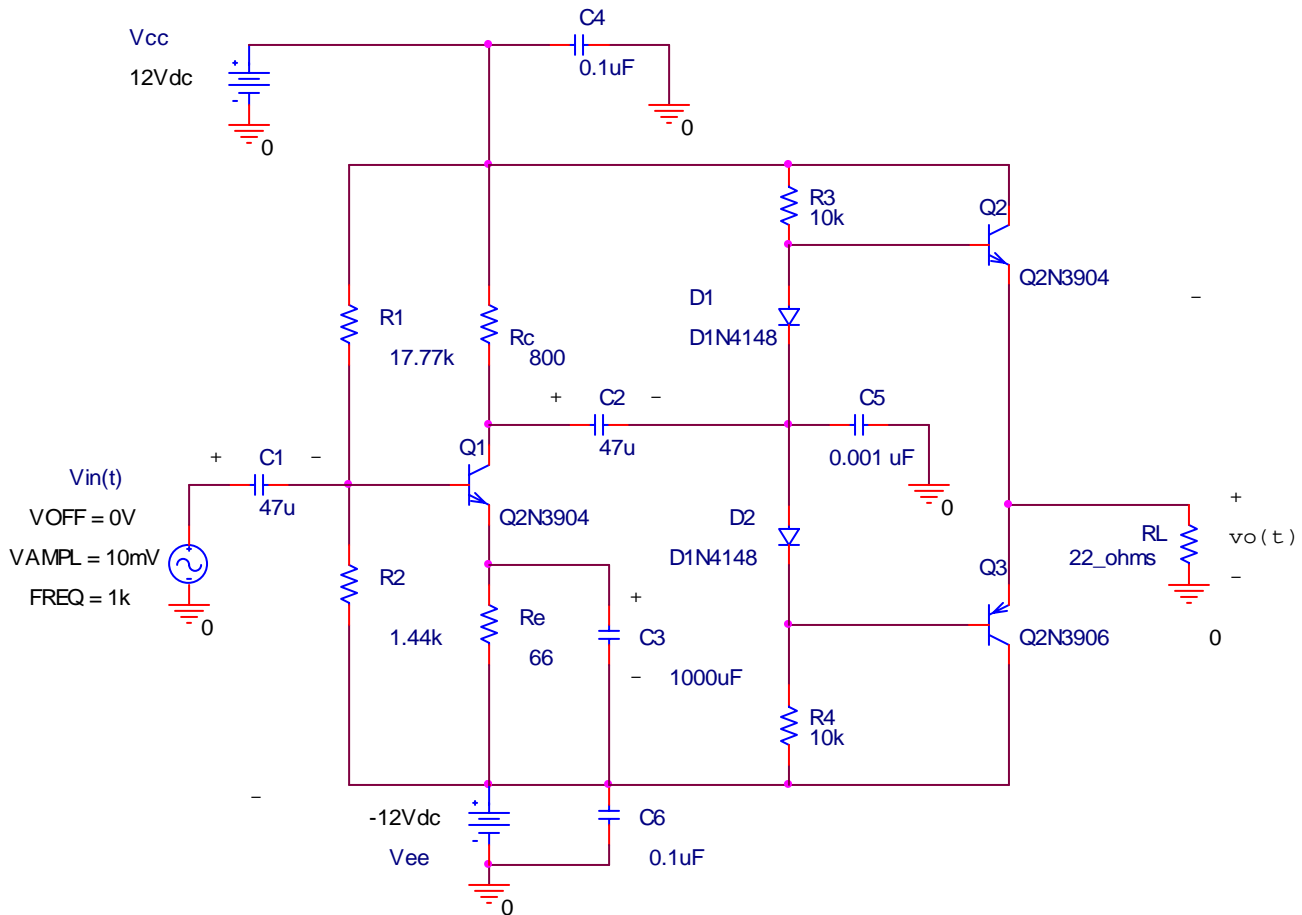
9. (***TO BE PERFORMED AS A CLASS DEMONSTRATION***!) Now consider the *complementary-symmetry* audio power amplifier circuit of Fig. 3. This power amplifier stage is used in virtually all modern audio amplifier circuits.

Note that this circuit uses your common-emitter (voltage) amplifier circuit from the previous laboratory project as the input stage for the circuit. For that reason, the resistor values in your first stage may differ slightly from those shown in Fig. 3.

The complementary-symmetry emitter follower output power amplifier stage is formed by NPN BJT Q2 and PNP BJT Q3. To get the circuit to function properly, Q2 and Q3 must have matched β's. To accomplish this, you will need to find a 2N3906 PNP BJT that has a β_F similar to that of the 2N3904 that you measured in part 1 of the lab. (Note that both transistors have the same pinout.)

Note that the curve tracer sets itself for tracing NPN BJTs by default upon power-up. This means that the curve tracer selects a positive-going Vce voltage scan, and a positively-stepped base current. When measuring the PNP BJT, you must set the curve tracer for the "negative going" Vce scan by operating the "Collector Supply Polarity" selector paddle located on the lower right panel of the curve tracer. Do this by changing the setting from "*Positive-going full-wave rectified sine wave*" to "*Negative-going full-wave rectified sine wave*". Note that making this change *also* automatically changes the base current step polarity from "*positive-going*" to "*negative-going*". Ideally, the β_F values of the two BJTs should be identical, so that the positive and negative excursions of the input signal are amplified equally. Compare how well matched your NPN and PNP BJTs are by calculating the percent deviation.

2N3904 (NPN) β_F = _____   2N3906 (PNP) β_F = _____

Percentage β_F match ((β_{NPN} - β_{PNP})/ β_{NPN})= _____%

To understand how this circuit works, assume that Q2 and Q3 have similar β_F values. RB1, RB2, D1, and D2 form a bias network, where the diodes are always on, and hence act like 0.6 V batteries. Thus the voltage at the base of Q2 is always 0.6 V *above* the input signal delivered to the junction of D1 and D2. Likewise, the voltage at the base of Q3 is always 0.7 V *below* the input signal. Likewise, the circuit symmetry suggests that the dc potential at the junction of the emitters of Q2 and Q3 is 0 V (ground potential). For zero signal input, D1 holds the base of NPN BJT Q2 at 0.6 V, therefore Q2 is *very lightly conducting* (near cutoff). Also, D2 holds the base of PNP BJT Q3 at –0.6 V, therefore Q3 is also *very lightly conducting* (near cutoff). But as the input signal (applied at the junction of D1 and D2) swings positive, the base voltages of Q2 and Q3 both rise, causing PNP BJT Q3 to turn off since Q3's emitter-base junction voltage falls below 0.6 V, and causing NPN BJT Q2 to conduct more heavily. Therefore, the NPN BJT Q2 functions as an emitter-follower during the positive half of the cycle, while Q3 is cut off, and is essentially not present. Because the emitter-follower exhibits essentially unity voltage gain, but with high input resistance and low output resistance, only a relatively small signal current is required from the common-emitter voltage amplifier stage (Q1) to drive a relatively large current into the low-impedance (loudspeaker) load. When the input signal goes negative, the situation is reversed, with NPN BJT Q2 now turning OFF, and the PNP BJT Q3 emitter-follower stage turning on. Now the task of driving the load has been "handed off" to Q3. Now Q3 acts as an emitter follower, allowing the negative portion of the signal to be delivered to the high current load, once again with very little drive current required from the voltage amplifier stage (Q1).

Build this circuit, using a 22 ohm resistor in place of the actual loudspeaker, and set the function generator to deliver a 10 mV peak-to-peak, 1 kHz sine wave. Carefully turn on the dc power while you monitor the Vcc = 9V and Vee = -9V dc power supply currents (they should remain less than 0.1 A) and feel the temperature of the transistors carefully with your finger. Be ready to remove your finger and turn off the power if either transistor becomes too hot to touch, and recheck your wiring!

10. (***TO BE PERFORMED AS A CLASS DEMONSTRATION***!) Connect the oscilloscope across the 22 ohm load resistor, and make sure that the output is a sine wave (with only a small amount of "cross-over" distortion, and that no appreciable high frequency oscillations are present in the output signal developed across RL. If they are, be sure that you have added 0.1 µF bypass capacitors between the +9V and -9V power busses and ground. ***As in the previous parts of this lab,, to avoid possible RF oscillations in your circuit, please "roll off" the high frequency voltage gain of the amplifier by connecting a 0.01 µF capacitor (see capacitor C5 in Fig. 3) between the collector of Q1 and ground in order to "short out" any possible high frequency signal oscillations, while still passing the desired audio frequencies.***

Recall the impedance of a 0.01 µF capacitor at the signal frequency (1 kHz) has a magnitude of 16 kΩ, so this capacitor should not interfere with circuit operation at the signal frequency. Try removing this capacitor and then reconnecting it, while observing the amplifier output signal waveform. Describe the results of this experiment in your lab report.

Measure the overall voltage gain of the system, Av = Vspeaker / Vfunction_generator. A 1-kHz tone should be audible in the loudspeaker. Capture a waveform from the oscilloscope showing both the input and output voltage with the 1kHz input. Make sure the scope capture includes measurements for the frequency of the input as well as the peak to peak value of the input and the output.

Experimentally determine the maximum symmetrical output voltage swing by gradually increasing the function generator voltage, while observing the voltage across the loudspeaker until either the positive or negative going portion of the sine wave begins to "flat-top". Capture a second oscilloscope picture at this point again showing the input and output voltage along with the same measures. Include both oscilloscope pictures as **Attachment D** in your lab writeup and record the key information from these plots in the table below. (I will provide Attachment D to each lab team, so you can incorporate it in your lab report.)

Record the observed overall voltage gain Av and also the maximum symmetrical swing in the blanks below:

Observed Av = _____

Max Symm Voltage Swing = _____ V, peak-peak

Replace the function generator with a microphone and the 22-ohm load resistor RL with an actual loudspeaker, and obtain the signature of the lab instructor certifying that your audio PA system amplifies speech with suitably high "fidelity". Take a look at the output from the speaker as you speak into the microphone to see the frequency content of your voice as an input.

11. PSPICE Simulation *(**To Be Performed by Each Team as part of your Lab Report!**)* Now perform a time domain (**transient**) PSPICE simulation of the circuit of Fig. 3. Note that you may want to flip (*ctrl-F*) and rotate (*ctrl-R*) one of the BJTs to properly orient it. Set your VSIN source for a frequency of 1 kHz and an amplitude of 10 mV.

When doing the assigned PSPICE simulation for Lab 7, you should NOT alter the BJT parameters for the Q2N3904 or the Q2N3906 model, except for changing the BF values to 100. The SPICE models for each of these BJTs should be:

.model Q2N3906   PNP(Is=1.41f Xti=3 Eg=1.11 Vaf=18.7 Bf=100 Ne=1.5 Ise=0
+   Ikf=80m Xtb=1.5 Br=4.977 Nc=2 Isc=0 Ikr=0 Rc=2.5 Cjc=9.728p
+   Mjc=.5776 Vjc=.75 Fc=.5 Cje=8.063p Mje=.3677 Vje=.75 Tr=33.42n
+   Tf=179.3p Itf=.4 Vtf=4 Xtf=6 Rb=10)

.model Q2N3904   NPN(Is=6.734f Xti=3 Eg=1.11 Vaf=74.03 Bf=100 Ne=1.259
+   Ise=6.734f Ikf=66.78m Xtb=1.5 Br=.7371 Nc=2 Isc=0 Ikr=0 Rc=1
+   Cjc=3.638p Mjc=.3085 Vjc=.75 Fc=.5 Cje=4.493p Mje=.2593 Vje=.75
+   Tr=239.5n Tf=301.2p Itf=.4 Vtf=4 Xtf=2 Rb=10)

The above simulation parameters should yield a simulated Av of around -160, which is still a bit higher than we measured in the lab using the demonstration circuit, but not too much larger.

From your PSPICE simulation, determine Av. Then re-simulate using progressively higher values of source amplitudes until you observe the output voltage waveform to begin to clearly flatten on one either the top or bottom end. From this distorted plot, determine the (simulated) maximum symmetrical output voltage swing. Be sure to include your PSPICE schematic and associated plots (the undistorted output voltage plot from which Av was measured and the distorted plot from which the maximum symmetrical output voltage swing was determined in **Attachment E**. Fill in your simulated results below, and find the % error between these simulated results and your experimental observations:

PSPICE Simulation results and the % deviation from the experimental observations

PSPICE: Av = _____   Observed Av = _____   %Error = _____;

Max Symm Vout Swing = _____Vpp,   Observed Value = _____   %Error = _____

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Attachment D. (ECE250 Lab Project 7) Vout and vin waveforms for 2-stage CE – CC complementary symmetry audio amplifier demonstration of Fig. 3. Waveforms recorded by Keith Hoover on 2/4/09.

Part A. Undistorted vout and vin waveforms. Av = vl/vin = 2.982/0.020 = 149.1
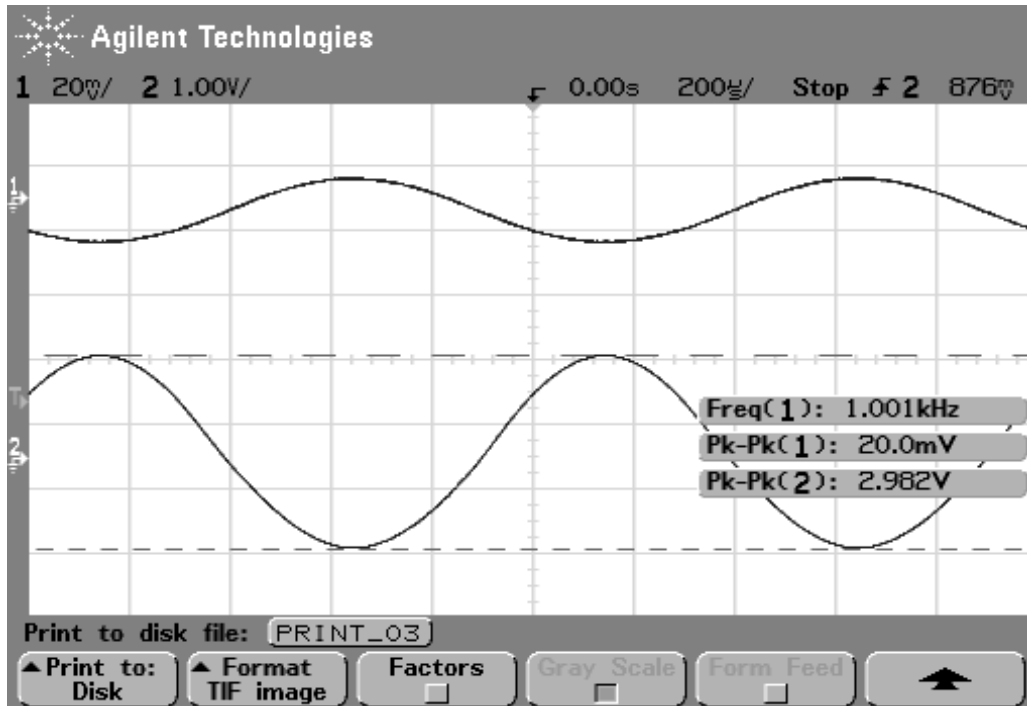
Part B. Distorted vout waveform (when vin amplitude is increased to a point just before vout badly flattens (on the bottom). Note the *maximum symmetrical swing* is approximately 4.54 V, peak-to-peak.