CSSE 332 -- Operating Systems

Multi-level Page Tables

Name: _____

Question 1. (10 points) Based on our discussion of a two-level page table with 16-bits addresses and 16-bit PTEs, draw how the following address would be used to lookup the corresponding physical address: `0x3D0B`.

Make sure to show your offset inside each page. Assume that the address of the first level page table is already provided in the appropriate register.

Question 2. (5 points) Describe the RISC-V organization of a 64-bit address to support multi-level page tables. Make sure to label each section of the address with its use in the address translation.

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Question 3. (5 points) In RISC-V, the address of the first level page table for every running process is stored in the _____ register.

Question 4. Assume we are dealing with `4 KB` pages in RISC-V with the address breakdown from **Question 2**. Answer the following questions.

(a) (5 points) How many page table entries (PTEs) does each page of the page table contain?

(b) (5 points) Given that, how wide if a PTE?

(c) (5 points) Describe the breakdown of a PTE into its corresponding constituents.