ADDITIONAL PROBLEM (ANALOG COMPUTER)

Ideal OP-AMP

P, node: \( \frac{V_i}{R_i} + 0 \cdot 0 = \Rightarrow V_i = 0 \)

N, node: \( V_o = V_i \leq 0 \)

\( 0 - V_{out} + 0 + \frac{d(0 - V_{in})}{dt} = 0 \)

\( V_{out} = -R_1C_1 \frac{dV_{in}}{dt} \)

4 Limitations: Your within limits of power supplies

\( \frac{dV_{in}}{dt} \) exists & defined

\( 1^{st} \) stage takes \( \frac{d}{dt} \) of input signal

In actual cases, a resistor would be placed in series with \( C_1 \) to limit "gain" at high frequencies
ADDITIONAL PROBLEM (ANALOG COMPUTER CONTINUED)

2nd stage (9-stage)

\[ V_{b1} + \frac{1}{C_0} \Rightarrow V_{b2} \approx 0 \]

\[ V_{b2} \approx 0 \]

\[ V_{in} = V_{in} \approx 0 \]

\[ V_{out} = \frac{R_2}{R_2} + 1 + \frac{C_2}{C_0} \frac{d}{dt} (V_{in} - V_{out}) + 0 \]

\[ \frac{dV_{out}}{dt} = -\frac{1}{R_2C_2} V_{out}, \]

\[ V_{out} = -\frac{R_2}{R_2C_2} \int V_{out} \, dt \]

C LIMITATIONS: \( V_{out} \) REMAINS WITHIN LIMITS OF POWER SUPPLIES

C USUALLY A RESISTOR WILL BE PLACED IN PARALLEL WITH THE CAPACITORS TO LIMIT THE "GAIN" FOR LOW FREQUENCIES

OVERALL LIMITING LIMITATIONS NARROW

\[ V_{out} \approx \frac{R_2C_1}{R_2C_2} V_{in} \]