ADDITIONAL PROBLEM DTL-WA40

Any input low will set \( V_x \) at 700 mV (\( V_{0x} \)).

For transistor to be on you need \( V_{BE} = V_{BEH} \).

For current to rise, \( V_0 \) must be 700 mV.

\( V_x \) max = 1.4V \( V \) will occur when both inputs are HIGH.

\[
\begin{array}{ccc}
\text{A} & \text{B} & \text{OUT} \\
\text{L} & \text{L} & \text{H} \\
\text{L} & \text{H} & \text{H} \\
\text{H} & \text{L} & \text{H} \\
\text{H} & \text{H} & \text{H} \\
\end{array}
\]

By design level when transistor is on should be \( V_{BE} \) sat (\( \approx 100 \text{ mV} \)).

A) For LOW output \( V_A = V_B = \text{HIGH} \).

\[
I_{R_B} = \frac{V_{CC} - V_x}{R_B} = \frac{5 - 1.4}{200} = 0.23 \text{ mA}
\]

\[
I_{BE} = \frac{V_{BEH}}{R_E} = \frac{0.7 - 5}{10} = 0.7 \text{ mA}
\]

\[
I_B = I_{R_B} - I_{BE} = 3.03 \text{ mA}
\]

Now for \( V_{0x} \leq 500 \text{ mV} \) \( I_E \approx 21 \text{ mA} \).
ADDITIONAL DTL PROBLEM CONTINUED

B) CONTINUED

Now for BJT to have \( V_c = V_{out} = 600 \text{ mV} \)

It must be actual

So \( I_c = \frac{8}{5} I_B \)

\[ I_c = 360 \text{ mA} \quad \text{(NOT REALISTIC BUT VALID #)} \]

\[ I_{load} = \text{into the collector from converter gates) must be the difference between } I_c \quad \text{and } I_c \]

\[ I_{load} = 360 \text{ mA} - 21 \text{ mA} \]

\[ = 339 \text{ mA} \]

Now for NICN output we have the BJT in circuit through the voltage drop \( (V_c - V_{out}) \)

If 24V must be due to current out through the load terminal since \( I_c = 0 \)

\[ I_{load, low output} \leq 339 \text{ mA} \quad \text{(for } \frac{V_c - V_{out}}{R_c} \text{)} \]

\[ I_{load, high output} \leq 12 \text{ mA} \]
Additional Problem (OTA NAND) continued

c) Since the transistor will either be on and saturated [(realistic values for I_
C < R_
L when I_
D < 2mA) → Therefore use inputs high output is low (saturated)] or
off and output is pulsed up toward VCC
the gate can be cascaded without
problems in level shifts.

→ Gate is Regenerative