Text Problems

5.1 [a) \( I_D = 3.06 \text{ mA} \); b) \( I_D = 2.81 \text{ mA} \)]
5.3 [a-i) \( I_D = 2.48 \text{ mA} \); a-ii) \( I_D = 6.88 \text{ mA} \); a-iii) \( I_D = 6.88 \text{ mA} \);
b-i) \( I_D = 4.68 \text{ mA} \); b-ii) \( I_D = 17.9 \text{ mA} \); b-iii) \( I_D = 22.3 \text{ mA} \)]
5.20 \( [V_{GS} = 3.62 \text{ V}, V_{DS} = 11.97 \text{ V}, I_D = 4.73 \text{ mA}] \)
D5.23 [various solutions possible, be sure to check your solution against required specifications]
5.27 \( [V_D = 3 \text{ V}, V_S = -1.72 \text{ V}] \)
5.35 [a) \( V_{GS1} = V_{GS2} = V_O = 2.5 \text{ V}, I_D = 1.73 \text{ mA} \); b) \( V_{GS1} = 2.09 \text{ V}, V_{GS2} = V_D = 2.91 \text{ V}, I_D = 1.00 \text{ mA} \)]

Additional Problems

1 Plot the graph of \( V_{out} \) (Y axis) vs. \( V_{in} \) (X axis) for the circuit shown in FIGURE 1 for five cases. The input voltage should sweep from 0 to 10 V. You should also plot the current from the power supply over the same input signal range. The MOSFET shown has a \( V_T \) of 2.5 V and a \( K(W/L) \) of 200 \( \mu \text{A/V}^2 \). The supply voltage (\( V_{DD} \)) is 10 V. Be careful to make sure the values used in ORCad for the MbreakN are correct – i.e. \( kp = 2*K(W/L) \). You should be able to do three of the cases at one time.
   A) The “LOAD” is replaced by a 5 k\( \Omega \) resistor.
   B) The “LOAD” is replaced by another MOSFET with the same characteristics as indicated above with the Gate terminal connected to the drain and the supply voltage (\( V_{DD} \)) and the source connected to the drain of the lower FET.
   C) The “LOAD” is replaced by a MOSFET connected as indicated in part B. The “LOAD” MOSFET has a \( K(W/L) \) 1/5 of the lower MOSFET but the same \( V_T \).
   D) The “LOAD” is replaced by a MOSFET connected as indicated in part B. The “LOAD” MOSFET has a \( K(W/L) \) 5 times that of the lower MOSFET but the same \( V_T \).
   E) The “LOAD” is replaced with a P channel MOSFET with \( V_T = -2.5 \text{ V} \) and \( K = 200 \text{ \ } \mu\text{A/V}^2 \). The Gate of the “LOAD” FET is connected to the Gate of the lower FET, the Source is connected to the power supply and the Drain is connected to the Drain of the lower FET.

2 Determine the load current flowing in the circuit shown in FIGURE 2 assuming all the FET’s are identical with \( V_{DD} = 10 \text{ V}, V_T = 2.5 \text{ V} \) and \( K = 4 \text{ mA/V}^2 \). What is the range of load resistance possible for this circuit to work correctly? Why? \([I_D = 25 \text{ mA}, P \leq 300 \Omega]\)