Pin List

1: VddIn  11: In  21: X  31: In
2: out2  12: X  22: clkOut  32: out5
4: out1  14: X  24: X  34: X
5: bias  15: chipGnd  25: chipVdd  35: padVdd
6: X  16: X  26: out6  36: X
7: X  17: X  27: GndOut  37: X
8: X  18: X  28: X  38: out4
9: In  19: GndIn  29: In  39: out3
10: X  20: X  30: X  40: X

Notes:
- chipVdd (25) and chipGnd (15) are used to power output buffers for out1:out6
- Vdd (1), chipVdd (25) and padVdd (35) may be connected together
- gnd (19) and chipGnd(15) may be connected together
- all In (9, 11, 29, 31) inputs may be connected together and then connected to a debounced digital switch
- bias (5) is used to bias output amplifiers embedded in voltage output pads
PinOut For Power/Ground Bounce Chip

Pin List

1: X 11: In 21: X 31: In
2: out2 12: X 22: clkOut 32: out5
4: out1 14: GndIn 24: X 34: X
5: bias 15: chipGnd 25: chipVdd 35: padVdd
6: X 16: VddIn 26: out6 36: X
7: X 17: X 27: GndOut 37: X
8: X 18: X 28: X 38: out4
9: In 19: X 29: In 39: out3
10: X 20: clkIn 30: X 40: clkIn

Notes:
• chipVdd (25) and chipGnd (15) are used to power output buffers for out1:out6
• chipVdd (25), padVdd (35), and VddIn (16) may be connected together
• GndIn (14) and chipGnd (15) may be connected together
• all In (9, 11, 29, 31) inputs may be connected together and then connected to a debounced digital switch
• bias (5) is used to bias output amplifiers embedded in voltage output pads
• both clkIn (20, 40) inputs may be connected together
## PinOut for Single Board to test Both Chips

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Notes:
- The pinout was chosen so that the same board can be used for either the clock skew lab or the power/ground bounce lab. The input to the flip-flops and the outputs are connected to the same pins for both chips.
- VddOut, GndOut, and clkOut are connected to the same pins for both chips.
- ClkIn, VddIn, and GndIn are connected to different pins for each chip.
- ChipVdd (25) and ChipGnd (15) are used to power output buffers for out1:out6.
- Vdd (1), ChipVdd (25), padVdd (35) and VddIn (16) may be connected together.
- Gnd (19), ChipGnd (15) and GndIn (14) may be connected together.
- All In (9, 11, 29, 31) inputs may be connected together and then connected to a debounced digital switch.
- Bias (5) is used to bias output amplifiers embedded in voltage output pads.
- All clkIn (13, 20, 40) inputs may be connected together.
The input ($In$) is a common connection to every flip-flop. Every flip-flop has an inverter in the cell. Power and the clock signal is routed as shown in the previous diagrams.