VIII.A. Astable Multivibrator

Design a 555 astable multivibrator (oscillator) circuit to achieve a frequency of oscillation of approximately 2 kHz. You may use only two resistors and two capacitors in your circuit. For timing applications never use electrolytic capacitors. Use standard 5% resistors available in your kit larger than 1 kΩ and a 5 V DC supply. Trace A of Figure VIII-1 shows an example of the waveform you should obtain.

- Draw a circuit schematic showing all connections and component values.
- Assuming that the 555 IC has no tolerance, resistors have ±5% tolerance, and capacitors have ±20% tolerance, calculate the minimum and maximum oscillation frequency of the circuit.
- In the lab, obtain a scope trace that shows the 555 output and the capacitor voltage. Show that the oscillation frequency is between the minimum and maximum frequencies calculated above. Show that the capacitor voltage oscillates between \( \frac{1}{3}V_{CC} \) and \( \frac{2}{3}V_{CC} \), where \( V_{CC} \) is your supply voltage.

VIII.B. 1 kHz 50% Duty-Cycle Oscillator

Hook the output of the 555 timer IC to the clock input of a J-K flip-flop to produce a 50% duty-cycle 1 kHz square wave. The J-K flip-flop should be wired so that it always toggles. Make sure that you hook up the clear and preset terminals of the J-K flip-flop so that they have no affect on the flip-flop. The number for a J-K flip-flop is 74xx76. The output of the J-K flip-flop should look like trace B in Figure VIII-1.

- Draw a circuit schematic showing all connections and component values.
- In the lab, obtain a scope trace that shows the 555 output and the J-K flip-flop output. Show that the frequency of the J-K flip-flop is 1 kHz.

VIII.C. One-Shot

Design a 74123 one-shot to produce a 100 µs pulse that is positive edge triggered. Use the output of the J-K flip-flop to trigger the one-shot. Hook up the clear input of the 74123 so that it has no effect. The output pulse should look as shown in trace C of Figure VIII-1. Note that the pulse starts at the rising edge of trace B, the J-K flip-flop output.

- Draw a circuit schematic showing all connections and component values.
- Assuming that the 74123 IC has no tolerance, resistors have ±5% tolerance, and capacitors have ±20 tolerance, calculate the minimum and maximum pulse width of the output pulse.
- In the lab, obtain a scope trace that shows the 74123 output and the J-K flip-flop output. Show that the pulse width is between the calculated minimum and maximum.
VIII.D. Summing Amplifier

Design an LM324 OPAMP circuit to implement the equation \( V_o = \frac{1}{2}(V_1 + V_2) \). The circuit should use a single supply so that the output of the LM324 can only go between 0 and 5 V. The summing amplifier should sum the output of the J-K flip-flop with the output of the 74123 to obtain a waveform similar to trace D of Figure VIII-1.

- Draw a circuit schematic showing all connections and component values.
- In the lab, obtain a scope trace that shows the output of the summing amplifier. Use the cursors to document the trace as necessary.

Figure VIII-1: Waveforms for Lab VIII.