1. (Modified Problem 11 on page 58 of Dr. Eccles' book) Implement
   \[ Z(A,B,C) = \Pi(0,2,3,7) \]
   using an 8-to-1 multiplexer.

2. Fill in K-map for function \( F(A,B,C,D) \) that is implemented by a 4-to-1 multiplexer and gates as in the following schematic.

3. (Multiplexer) Implement the 2-bit unsigned-number half subtractor
   Homework #9 with 74LS151 multiplexer chips and necessary gates. The four inputs are \( X=X_1X_0 \) and \( Y=Y_1Y_0 \). The outputs are two-bit difference \( D=D_1D_0 \) and one-bit borrow \( B \). \( X_1X_0 - Y_1Y_0 = D_1D_0 .... \)
   B. Borrow occurs when \( X<Y \).

   Simulate your design with LogicWorks 4. Submit both your circuit schematic and annotated waveforms with zero gate delay.