

## 2 Theory of an Analog Phase-Locked Loop (PLL)

### 2.1 Overview

A phase-locked loop is a feedback controlled circuit that maintains a constant phase difference between a reference signal and an oscillator output signal.

### 2.2 General Operation of a PLL

Figure 1 shows a basic block diagram of a PLL. A phase frequency detector compares the phase of the VCO output frequency,  $f_{osc}$ , with the phase of a reference signal frequency,  $f_{ref}$ . A phase detector output pulse is generated in proportion to that phase difference. This pulse is smoothed by passing it through a loop filter. The resulting dc component is used as the input voltage for controlling the VCO. The output of the VCO,  $f_{osc}$ , is fed back to the phase frequency detector input for comparison which in turn controls the VCO oscillating frequency to minimize the phase difference. Therefore, both frequency and phase are made the same, i.e.,  $f_{osc} = f_{ref}$  and  $\theta_{osc} = \theta_{ref}$ , such that the phase and frequency of the VCO and the reference signal source are in a locked state.

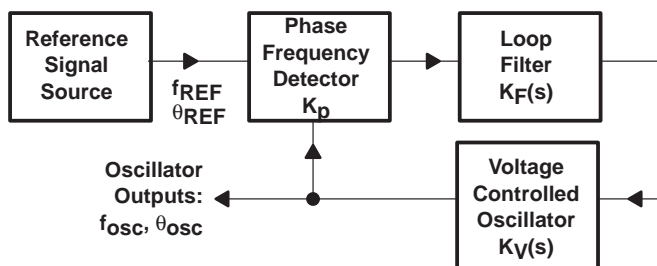


Figure 1. Basic PLL Block Diagram

Therefore, the PLL is a negative feedback circuit which compares the current value to a reference value to make the difference as close to zero as possible.

#### 2.2.1 Analysis of a PLL as a Feedback Control System

An analysis can be performed using the linearized block diagram in Figure 2.

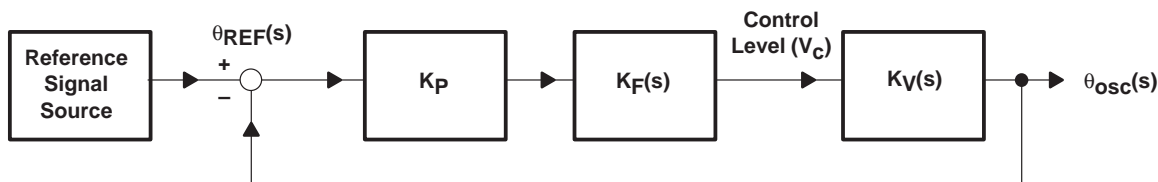


Figure 2. Linearized PLL Block Diagram

The parameters in Figure 2 are defined as follows:

- $K_P$  = gain of the phase frequency detector (V/rad)
- $K_F$  = transfer function of the loop filter (V/V)
- $V_C$  = VCO control level
- $V_C$  = VCO control level
- $s$  = Laplace variable

Using a Laplace transform, the closed-loop transfer function can be expressed as:

$$\frac{\theta_{osc}(s)}{\theta_{REF}(s)} = \frac{K_P \times K_F(s) \times K_V(s)}{1 + K_P \times K_F(s) \times K_V(s)} = W(s) \quad (1)$$

The VCO transform gain,  $K_V$ , is a function of time. Since phase is the time integral of frequency, the gain can be expressed as follows:

$$K_V(s) = \frac{K_V}{s} \quad (2)$$

The phase frequency detector gain is assumed to not to be a function of frequency.

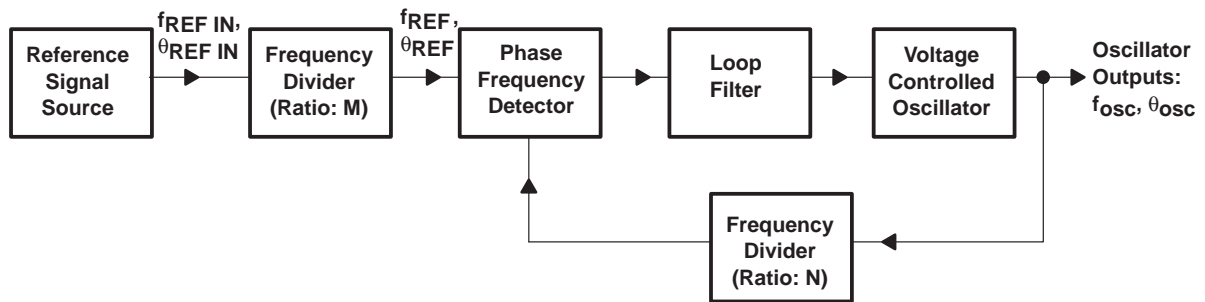
From equation 1 and equation 2

$$W(s) = \frac{K_P \times K_F(s) \times K_V}{s + K_P \times K_F(s) \times K_V} \quad (3)$$

This equation is the general linear transfer function for a PLL.

The PLL has become widely used as a frequency synthesizer by generating frequencies from a single reference signal source such as a crystal oscillator.

Consider the operation of the PLL frequency synthesizer in Figure 3.



**Figure 3. PLL Frequency Synthesizer Block Diagram**

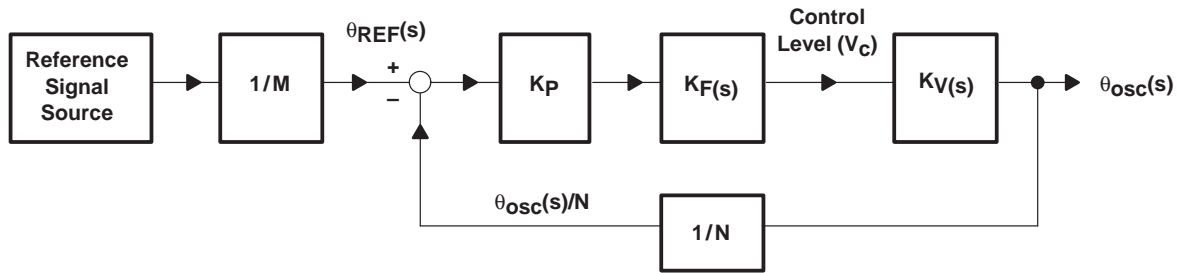
Since the signal from the reference signal source is used to generate the desired frequency in a frequency synthesizer, only frequencies at multiples of the reference frequency can be obtained.

The phase frequency detector compares the signal from the  $1/N$  frequency divider which divides the output signal of the VCO, and the signal from the  $1/M$  frequency divider which divides the output signal of the reference signal source, and controls the VCO frequency in such a way so that both frequency and phase are the same.

$$\text{Therefore, } \frac{f_{refin}}{M} = \frac{f_{osc}}{N} \quad (4)$$

$$\text{and the oscillating frequency, } f_{osc} = f_{refin} \times \frac{N}{M} \quad (5)$$

The closed-loop transfer function of the PLL in equation 1 can now be considered. If  $1/M$  and  $1/N$  frequency dividers are inserted into the block diagram of Figure 3, then Figure 2 becomes Figure 4.



**Figure 4. Linearized PLL Frequency Synthesizer Block Diagram**

Thus, the closed-loop transfer function can be expressed by the following equation:

$$W(s) = \frac{K_P \times K_F(s) \times K_V}{s + \frac{K_P \times K_F(s) \times K_V}{N}} \quad (6)$$

If the multiplication parameter  $N$  is set to 1 in equation 6, it becomes equation 3.

In this application report, equation 6 is used as the closed-loop transfer function for the PLL.

From equations 3 and 6, the closed-loop transfer function of the PLL is heavily dependent on the characteristics of the loop filter which is discussed later in this application report.

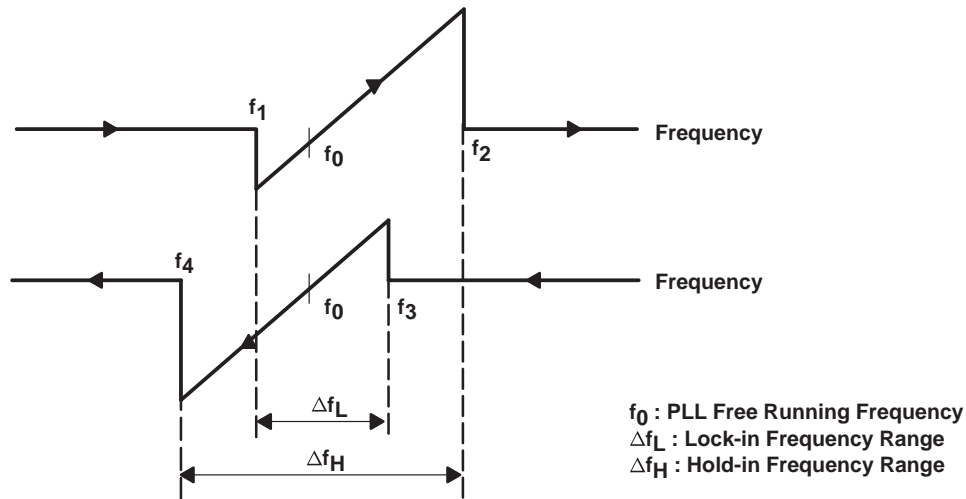
## 2.2.2 Definitions

### 2.2.2.1 Free Running Frequency

The free oscillating frequency of the VCO when it is in an unlocked state is called the free running frequency.

### 2.2.2.2 Hold-In Range (Lock Range) and Lock-In Range (Capture Range)

When the PLL is in the phase-locked state, the frequency range in which the frequency of the input reference signal,  $f_{REF}$ , can slowly be pulled away from the free running frequency of the VCO but still maintain the phase-locked condition is called the hold-in range or lock range. When the PLL is not in the phase-locked state, if the frequency of the input signal,  $f_{REF}$ , slowly approaches the free running frequency of the VCO, the frequency range in which the input signal becomes phase-locked is called the lock-in range or capture range.



**Figure 5. Concept Behind Hold-In Range and Lock-In Range**

Referring to the conceptual diagram in Figure 5, if the input signal frequency is increased slowly from a very low frequency not phase-locked to the VCO free running frequency, phase-lock occurs at frequency  $f_1$ . If the input signal frequency continually increases, it will pass through the free running frequency and then become unlocked at frequency  $f_2$ . Conversely, if the input signal frequency is decreased slowly from a very high frequency not phase-locked to the VCO free running frequency, phase lock occurs at frequency  $f_3$ . If the input signal frequency continually increases, it will pass through the free running frequency and the PLL becomes unlocked at frequency  $f_4$ . The hold-in range,  $\Delta f_H$ , and lock-in range,  $\Delta f_L$ , can be expressed as the following equations:

$$\Delta f_H = (f_2 - f_4) \quad (7)$$

$$\Delta f_L = (f_3 - f_1) \quad (8)$$

Normally, the relationship of  $\Delta f_H > \Delta f_L$  exists.

### 2.2.2.3 Lock-Up Time (Acquisition Time)

The amount of time required for the loop to phase lock is called lock-up time or acquisition time.

## 2.3 PLL Functional Blocks

### 2.3.1 Voltage-Controlled Oscillator (VCO)

The VCO is an oscillator circuit with the following characteristics whose output frequency is controlled by a voltage.

- $K_V$  = VCO gain (rad/V/sec) from Section 2.2.1
- Stable with respect to external disturbances (change in voltage, temperature, etc.)
- Control voltage versus oscillating frequency should ideally be linear
- Frequency adjustment should be simple

Because it is extremely difficult to satisfy all these conditions at the same time, a suitable oscillator should be chosen based on the application.

Oscillators that are typically used include the following:

- Crystal oscillator
- LC oscillator
- CR oscillator

For a VCO utilizing any of the above oscillation techniques, many excellent technical books and articles on VCO circuit design should be used.

### 2.3.2 Phase Detector Operation and Types

A phase detector detects phase differences between two input signals and produces a voltage based on this phase difference.

Phase detectors can be either analog or digital. For analog, representative devices are ring modulators and multipliers which are also called double balanced mixers. For digital, representative devices are OR-gates, ExOR-gates, RS flip-flops, 3-state buffers, and phase frequency detectors.

Only the digital phase detectors are discussed in this application report.

#### 2.3.2.1 OR-Gate Type Phase Detector

The simplest form of digital type phase detectors is the OR-gate type shown in Figure 6(a).

For an OR-gate type phase detector, the output signal duty cycle varies depending on the phase difference as shown in Figure 6(b). Then this output signal is smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 6(c).

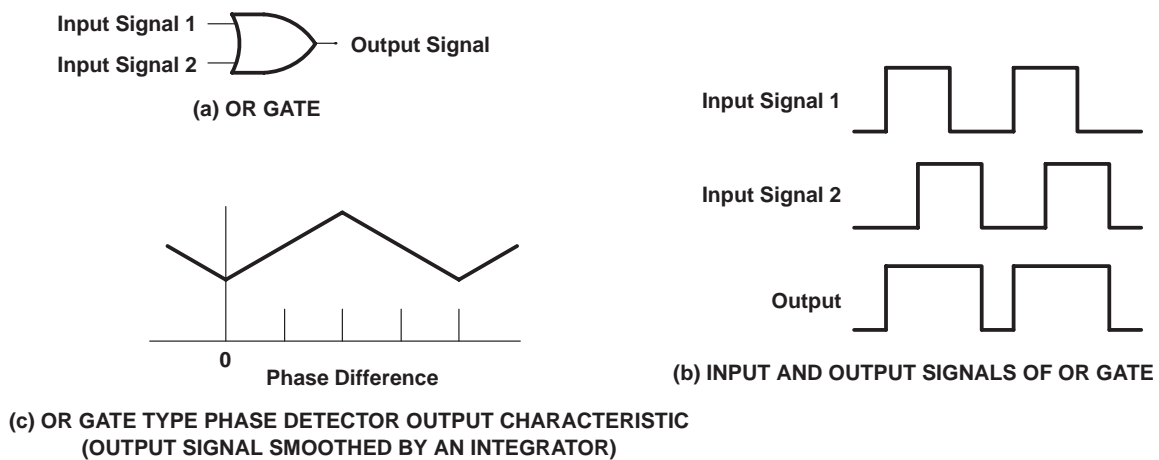
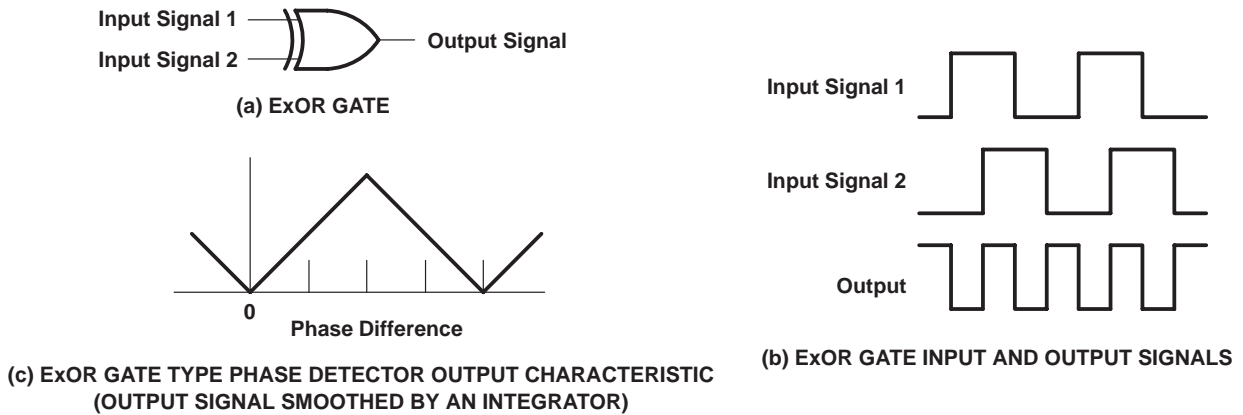


Figure 6. OR-Gate Type Phase Detector

#### 2.3.2.2 ExOR-Gate Type Phase Detector

An ExOR gate phase detector is shown in Figure 7(a).



**Figure 7. ExOR-Gate Type Phase Detector**

For this type of phase detector, the duty cycle of the output signal varies depending on the phase difference as shown in Figure 7(b). This output signal is also smoothed by an integrator. The resulting output voltage in relation to the phase difference is shown in Figure 7(c).

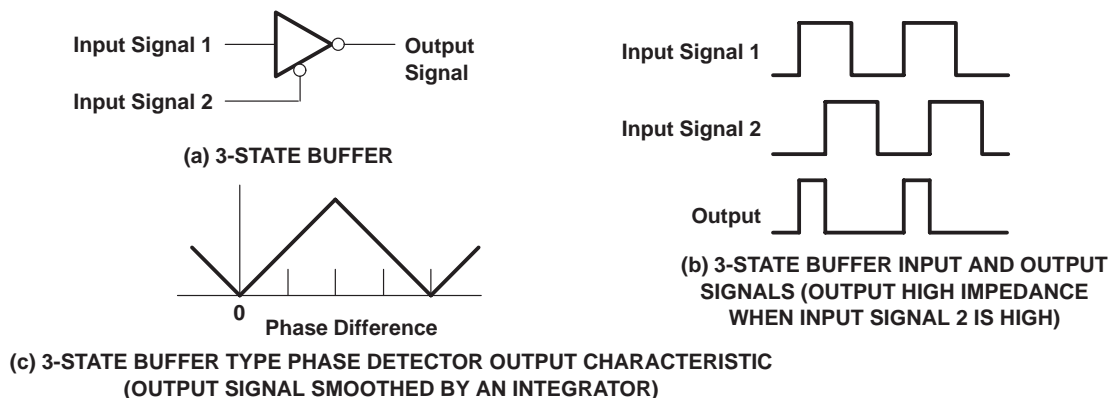
For this ExOR-gate type of phase detector, as compared to an OR-gate type of phase detector, the integrator output signal swings from 0 V to the supply voltage,  $V_{DD}$ . Moreover, because the ExOR-gate output frequency is twice that of the OR-gate, the high frequency components are more easily filtered out by the integrator.

However, when using an ExOR-gate as a phase detector, if each input signal duty cycle is not 50%, the output voltage generated from the phase difference does not have acceptable linear characteristics. Therefore, care must be exercised when using this type of phase detector.

### 2.3.2.3 3-State Buffer Type Phase Detector

A 3-state buffer type phase detector is shown in Figure 8(a).

The 3-state buffer phase detector output characteristic, as shown in Figure 8(c), is basically the same as ExOR gate phase detector. However, when input signal 2 is high, the output is in a high impedance state as shown in Figure 8(b).



**Figure 8. 3-State Buffer Type Phase Detector**

### 2.3.2.4 Reset-Set Flip-Flop Type Phase Detector

A Reset-Set flip-flop phase detector is shown in Figure 9, and the input and output signals are shown in Figure 9(b).

As shown in Figure 9(c), a RS flip-flop type phase detector has twice the comparison range of an ExOR gate type phase detector.

The R-S flip-flop type phase detector can be constructed using only an R-S flip flop. The pulse width of the input signal pulses is small, so a SET-RESET error difference do not cause a significant error. This condition can be solved by inserting AND-gates as shown in Figure 9(a).

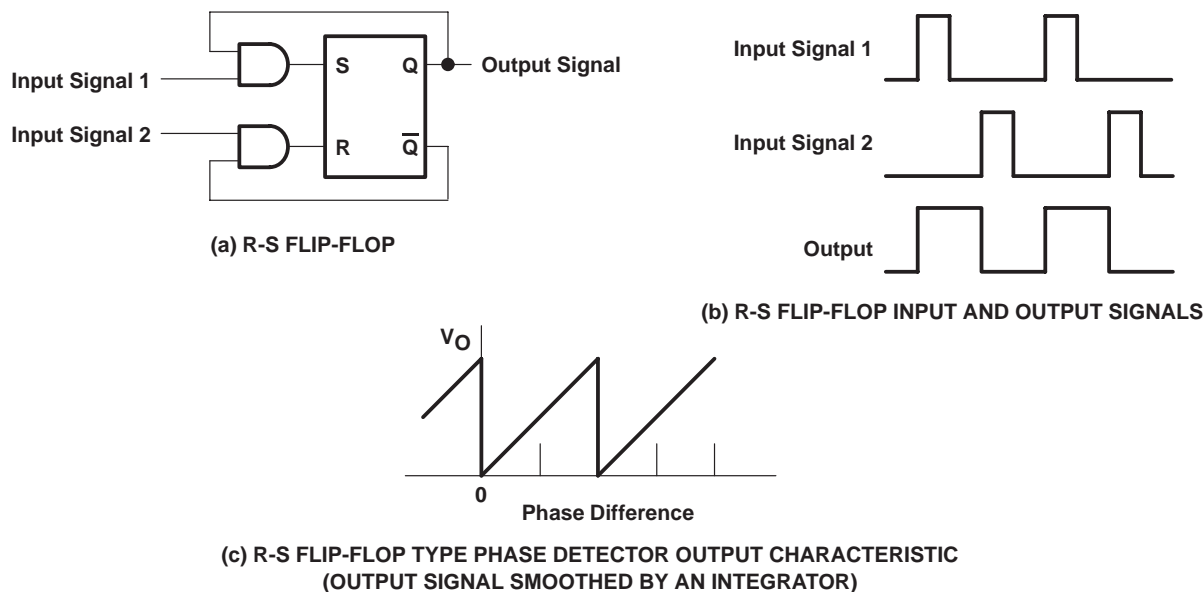


Figure 9. RS Flip-Flop Type Phase Detector

### 2.3.2.5 Phase Frequency Detector (PFD)

Of the phase detectors currently available, the most commonly used in a PLL is a circuit called a phase frequency detector. Figure 10(a) shows an example of a phase frequency detector.

In Figure 10(b), when the input signal 2 phase lags that of input signal 1, phase detector output D goes high starting from the rising edge of input signal 1 to the rising edge of input signal 2, that is, during the period of time corresponding to a phase difference between inputs 1 and 2, output D goes high. During this same period, output U stays low. When the phase of input 2 leads that of input 1, output D stays low from the rising edge of input 2 to the rising edge of input 1. During that time, U goes high.

When both inputs 1 and 2 have the same phase, both outputs D and U stay low. Depending on the phase detector outputs D and U, the charge pump MOS transistors are turned on and off resulting in output levels of  $V_{OH}$ ,  $V_{OL}$ , or high impedance. So when D is high and U is low, the MOS transistor  $Q_1$  is on and  $Q_2$  is off, therefore, the output level is  $V_{OH}$ . When U is high and D is low,  $Q_2$  is on and  $Q_1$  is off, resulting in the output level of  $V_{OL}$ . When both D and U are low,  $Q_1$  and  $Q_2$  are both off and the output becomes high impedance.

In this way, the output level is proportional to the phase difference. The output signal characteristic is shown in Figure 10(c).

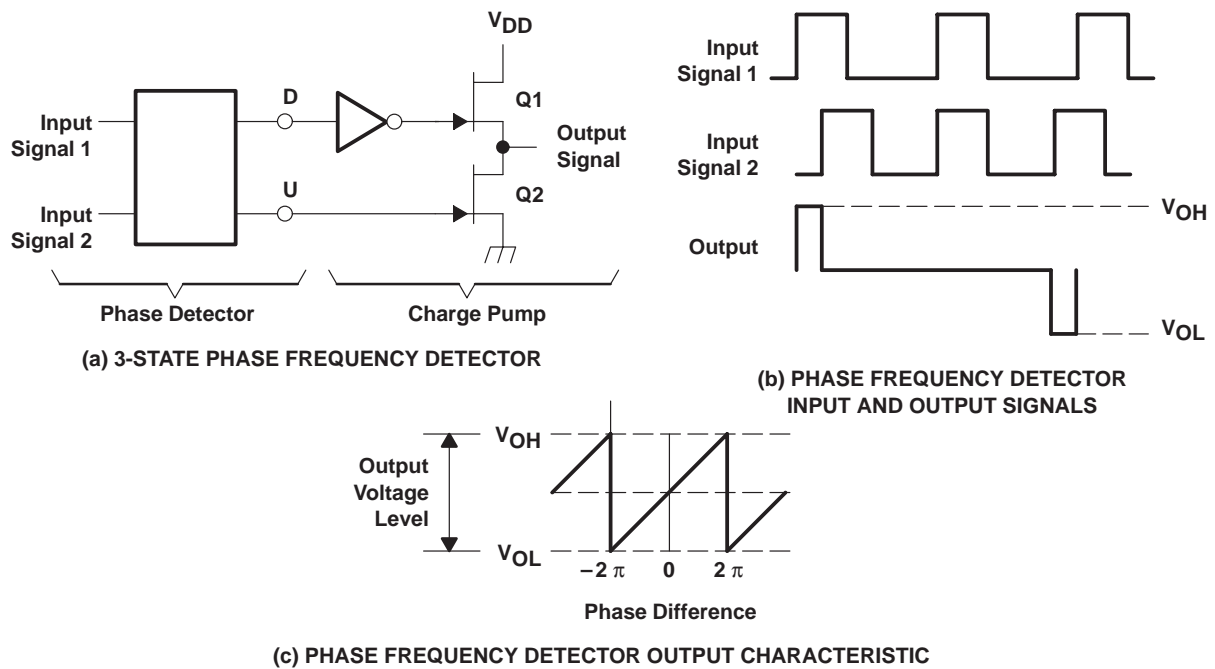


Figure 10. 3-State Phase Frequency Detector

## 2.4 Loop Filter

The loop filter smooths the output pulses of the phase detector and the resulting dc component is the VCO input. From the closed-loop transfer function (equation 6) obviously the loop filter is very important in determining the characteristics of the PLL response.

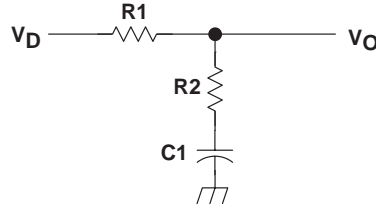
Some examples of a loop filter are a lag filter, a lag-lead filter, and an active filter. Among these, the most commonly used are the lag-lead filter and the active filter. For these two filters, the PLL closed loop transfer functions are derived, and design examples for the filter parameters are shown.

## 2.5 Transfer Function Using a Lag-Lead Filter

First, the lag-lead filter transfer function is derived from Figure 11. If a Laplace transform is taken, then

$$\frac{V_o}{V_D} = K_F(s) = \frac{1 + sC1 \times R2}{1 + sC1(R1 + R2)} = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_r)} \quad (9)$$

$$\text{Where:} \quad \tau_1 = C1 \times R1, \quad \tau_2 = C1 \times R2 \quad (10)$$



**Figure 11. Lag-Lead Filter**

By substituting equation 9 into equation 6 and rearranging the terms, the PLL closed-loop transfer function is

$$W(s) = \frac{1 + s\tau_2}{\left\{(\tau_1 + \tau_2)/K\right\} \times s^2 + \left\{(N + K \times \tau_2)/(N \times K)\right\} \times s + 1/N} \quad (11)$$

Where:

$$K_P \times K_V = K \quad (12)$$

If this equation is further expanded, it becomes

$$\begin{aligned} W(s) &= W_1(s) + W_2(s) \quad (13) \\ &= \frac{1}{\left\{(\tau_1 + \tau_2)/K\right\} \times s^2 + \left\{(N + K \times \tau_2)/(N \times K)\right\} \times s + 1/N} \\ &\quad + \frac{s\tau_2}{\left\{(\tau_1 + \tau_2)/K\right\} \times s^2 + \left\{(N + K \times \tau_2)/(N \times K)\right\} \times s + 1/N} \end{aligned}$$

The general transfer function for a second order system is shown below

$$G(s) = \frac{1}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \quad (14)$$

Where:

$\omega_n$  is the natural angular frequency and  $\zeta$  is the damping factor.

If, in equation 15 the right hand side first term is designated as  $W_1(s)$  and the second term as  $W_2(s)$ , then  $W_1(s)$  is a second order system as in equation 14 and  $W_2(s)$  is a second order lag with gain of  $\tau_2$  multiplied by  $s$ .

If  $W_1(s)$  is equated to equation 14 and the coefficients compared

$$\begin{aligned} W_1(s) &= \frac{1 + s\tau_2}{\left\{(\tau_1 + \tau_2)/K\right\} \times s^2 + \left\{(N + K \times \tau_2)/(N \times K)\right\} \times s + 1/N} \quad (15) \\ &= \frac{1}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \end{aligned}$$

the following are derived:

$$\omega_n = \sqrt{\frac{K}{N(\tau_1 + \tau_2)}} \quad (16)$$

$$\zeta = \frac{1 + K\tau_2}{2\sqrt{N(\tau_1 + \tau_2)} \times K} = \frac{\omega_n}{2} \left( \tau_2 + \frac{N}{K} \right) \quad (17)$$

Similarly for  $W_2(s)$ :

$$\begin{aligned} W_2(s) &= \frac{s\tau_2}{\left\{ (\tau_1 + \tau_2)/K \right\} \times s^2 + \left\{ (N + K \times \tau_2)/(N \times K) \right\} \times s + 1/N} \\ &= \frac{(2\zeta/\omega_n - N/K) \times s}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \end{aligned} \quad (18)$$

Thus, using a lag-lead filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n - N/K) \times s}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \quad (19)$$

From the above result, design equations for lag-lead filter parameters are derived.

If  $\tau_1 = C1 \times R1$  and  $\tau_2 = C2 \times R2$  are substituted into equations 16 and 17 respectively and solved for  $R1$  and  $R2$ , the following equations are derived:

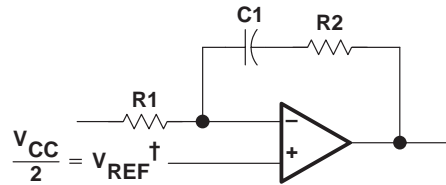
$$R1 = \left( \frac{K}{\omega_n^2} \times \frac{1}{N} - \frac{2\zeta}{\omega_n} + \frac{N}{K} \right) \times \frac{1}{C1} \quad (20)$$

$$R2 = \left( \frac{2\zeta}{\omega_n} - \frac{N}{K} \right) \times \frac{1}{C1} \quad (21)$$

## 2.6 Transfer Function Using an Active Filter

When using an active filter, the PLL closed-loop transfer function and design equation for filter parameters are derived in the same fashion as in Section 2.5.

First, the Laplace transform is taken and the transfer function of an active filter is derived. Figure 12 shows an example of an active filter.



† Voltage used for single ended power supply systems.

**Figure 12. Active Filter**

The transfer function for the active filter is

$$K_F(s) = \frac{1 + sC1 \times R2}{sC1(R1 + R2)} = \frac{1 + s\tau_2}{s\tau_1} \quad (22)$$

Where:

$$\tau_1 = C1 \times R1 \text{ and } \tau_2 = C1 \times R2 \quad (23)$$

From the PLL closed-loop transfer function, if  $K_F(s)$  is substituted into equation 6 and equation 6 is simplified, it becomes

$$W(s) = \frac{1 + s\tau_2}{(\tau_1/K) \times s^2 + (\tau_2/N) \times s + 1/N} \quad (24)$$

Where:

$$K_P \times K_V = K \text{ as before.} \quad (25)$$

If this equation is expanded further, it becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1}{(\tau_1/K) \times s^2 + (\tau_2/N) \times s + 1/N} + \frac{s\tau_2}{(\tau_1/K) \times s^2 + (\tau_2/N) \times s + 1/N} \quad (26)$$

As shown before, second order lag resonators can be expressed as equation 14.

Following the procedure in Section 2.5.

If  $W_1(s)$  is equated to equation 14

$$W_1(s) = \frac{1}{(\tau_1/K) \times s^2 + (\tau_2/N) \times s + 1/N} = \frac{1}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \quad (27)$$

the following are derived:

$$\omega_n = \sqrt{\frac{K}{N\tau_1}} \quad (28)$$

$$\zeta = \frac{\tau_2}{2N} = \sqrt{\tau_1/(N/K)} = \frac{\omega_n}{2} \tau_2 \quad (29)$$

Similarly for  $W_2(s)$ :

$$W_2(s) = \frac{s\tau_2}{(\tau_1/K) \times s^2 + (\tau_2/N) \times s + 1/N} = \frac{(2\zeta/\omega_n) \times s}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \quad (30)$$

Thus for the active filter, the PLL closed-loop transfer function becomes

$$W(s) = W_1(s) + W_2(s) = \frac{1 + (2\zeta/\omega_n) \times s}{(1/\omega_n^2) \times s^2 + (2\zeta/\omega_n) \times s + 1} \quad (31)$$

From the above result, the design equation for active filter parameters can be derived.

If  $\tau_1 = C1 \times R1$  and  $\tau_2 = C1 \times R2$  are substituted into equations 28 and 29 respectively, and solved for  $R1$  and  $R2$ , the following two equations are derived:

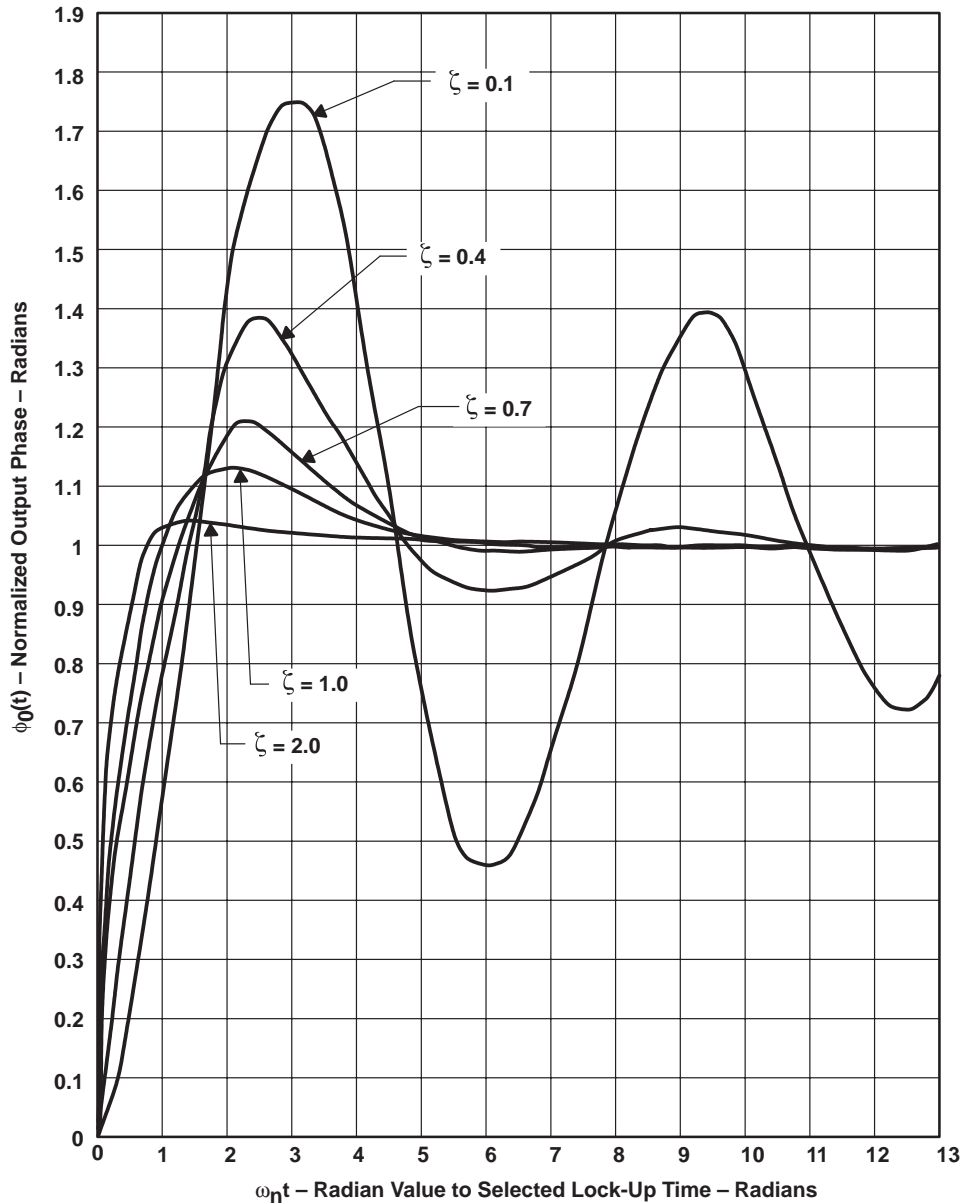
$$R1 = \frac{K}{\omega_n^2} \times \frac{1}{N} \times \frac{1}{C1} \quad (32)$$

$$R2 = \frac{2\zeta}{\omega_n} \times \frac{1}{C1} \quad (33)$$

## 2.7 General Design Procedures

Based on a PLL step response, the damping factor can be chosen, the natural angular frequency can be evaluated, and the characteristics of response time and relative stability can be examined. For the PLL transfer function in equation 31, the step responses of several cases are shown in Figure 13. As shown, the smaller the  $\zeta$  value the larger the ringing, and a large  $\zeta$  value results in little or no ringing. Also, a larger  $\omega_n$  results in a faster response time.

The step response for a PLL using an active filter as a loop filter is shown in Figure 13. When a passive lag-lead filter is used, if the condition  $\omega_n \ll K/N$  is met for equation 19, the step response is similar to the step response shown.



**Figure 13. PLL Step Response Using the Active Filter in Figure 17**

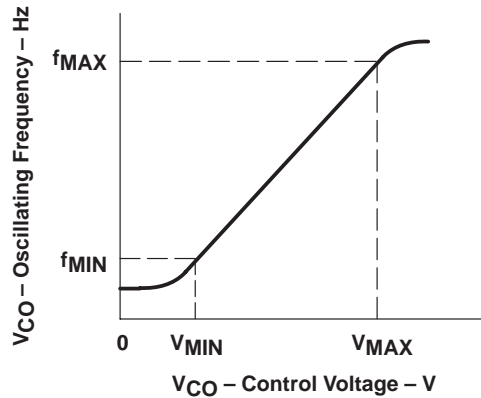
To design a PLL system,  $\zeta$  is selected first. Then from the step response characteristic, the value of  $\omega_n t$ , at which the response is decayed to within 5% of the final value, is found. Then  $\omega_n t$  is divided by the desired lock-up time,  $t_s$ , to determine  $\omega_n$ . The following steps should be followed.

1.  $\zeta$  is a measure of stability. and usually  $\zeta$  is selected to be between value of 0.6 to 0.8.
2. Assume  $\zeta$  is selected to be a value of 0.7.
3. The value of  $\omega_n t$  from the step response characteristic is determined to be 4.5 for response settling within 5%.
4. Lock-up time,  $t_s$ , is determined by system requirements.
5. The PLL natural angular frequency,  $\omega_n$ , is

$$\omega_n = \frac{\omega_{n^r}}{t_s} = \frac{4.5}{t_s} \text{ (rad/sec)} \quad (34)$$

This criterion varies depending on the system application. It is appropriate to pick the natural frequency ( $f_n = \omega_n/2\pi$ ) to be one tenth to one hundredth of the reference frequency of the phase frequency detector.

6. The frequency division ratio is determined from the reference frequency and the desired frequency according to equation 5.
7. Determine the VCO gain parameter,  $K_V$ . An example of a VCO oscillating frequency characteristic is shown in Figure 14.



**Figure 14. VCO Oscillating Frequency Characteristic**

From the oscillating frequency characteristic of Figure 14, the VCO gain can be determined using the following equation:

$$K_V = \frac{f_{MAX} - f_{MIN}}{V_{MAX} - V_{MIN}} \times 2\pi \text{ [rad/sec/V]} \quad (35)$$

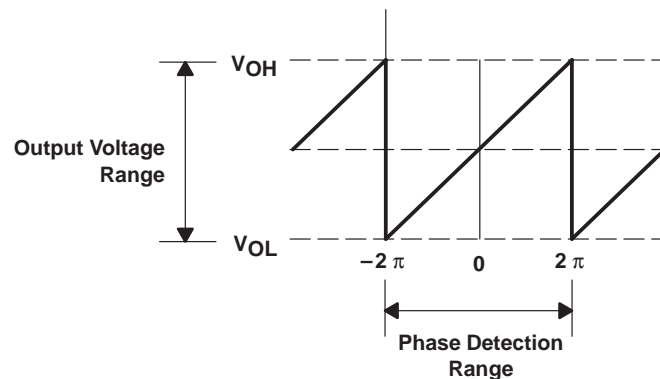
Where:

$f_{MAX}$  = maximum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

$f_{MIN}$  = minimum frequency at which the linearity of the oscillating frequency versus the VCO control voltage can be maintained.

$V_{MAX}$  = control voltage at which the VCO oscillating frequency is  $f_{MAX}$

$V_{MIN}$  = control voltage at which the VCO oscillating frequency is  $f_{MIN}$



**Figure 15. Phase Frequency Detector Output Characteristic**

8. Determine the phase detector gain parameter,  $K_P$

Based on the phase frequency detector output characteristic in Figure 15, the phase detector gain can be determined from equation 34.

$$K_P = \frac{V_{OH} - V_{OL}}{4\pi} \quad [V/rad] \quad (36)$$

Where:

$V_{OH}$  = maximum output voltage

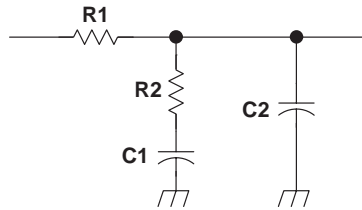
$V_{OL}$  = minimum output voltage

For other types of phase detectors, the phase detector gain can be determined in the same fashion.

9. Filter parameters can be determined by substituting each of the values determined in steps 1 through 8 into the corresponding equations.

For the lag-lead filter, substituting the desired values of  $\omega_n$ ,  $\zeta$ ,  $N$ , and  $K$  into equations 20 and 21, the filter parameters can be determined by choosing an appropriate value for  $C1$ .

For a practical loop filter, a second order lag-lead filter with an additional capacitor  $C2$ , as shown in Figure 16, to minimize spurious noise at the VCO input should be used.



**Figure 16. Lag-Lead Filter (With Additional Capacitor)**

The value of  $C2$  should be less than or equal to  $C1/10$  to keep  $C2$  from affecting the low-pass filter response while providing adequate noise filtering.

Similarly for the case of an active filter, substituting the desired values of  $\omega_n$ ,  $\zeta$ ,  $N$ , and  $K$  into equations 32 and 33, the filter parameters can be determined by choosing an appropriate value for  $C1$ .

Also when using an active filter as the loop filter, as shown in Figure 17, a second order active filter with one additional capacitor should be used.

The additional capacitor  $C2$  is used for compensating the  $R2$  high frequency response. The cutoff frequency,  $\omega_c$ , of  $C2$  and  $R2$  should be chosen to be ten times that of the natural frequency,  $\omega_n$ , of the PLL.

$$\omega_c = \frac{1}{(C2 \times R2)} \cong 10\omega_n \quad (37)$$

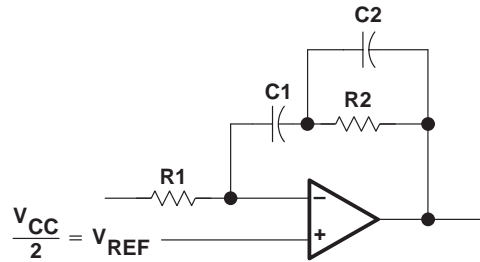


Figure 17. Active Filter (With Additional Capacitor)

## 2.8 Frequency Division

When given an input signal with frequency  $f$ , a circuit that generates a  $f/N$  ( $N$  an integer) signal synchronized to the input signal is called a frequency divider. Usually frequency dividers use programmable counters like the one shown in Figure 18 (programmable meaning that the frequency divide ratio  $N$  can be changed and controlled externally).

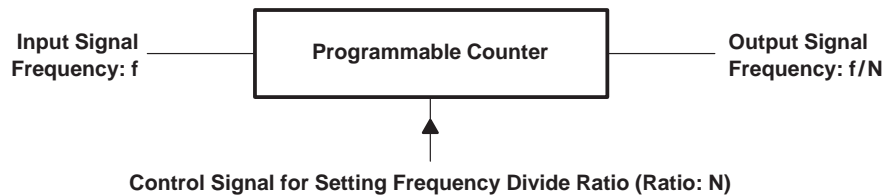


Figure 18. Programmable Counter

The construction of a PLL frequency divider using a programmable counter, and the prescaler and pulse swallow methods (2s modulus prescaler method) are discussed in the following sections.

### 2.8.1 Prescaler Method

If the frequency,  $f$ , of an input signal is too high, a divide can be added using an additional programmable counter in the feedback path. As shown in Figure 19, the frequency can be divided before the programmable counter using a fixed frequency divider (prescaler) operating at high speed, this lowers the input frequency to the programmable counter. This method is called the prescaler method.

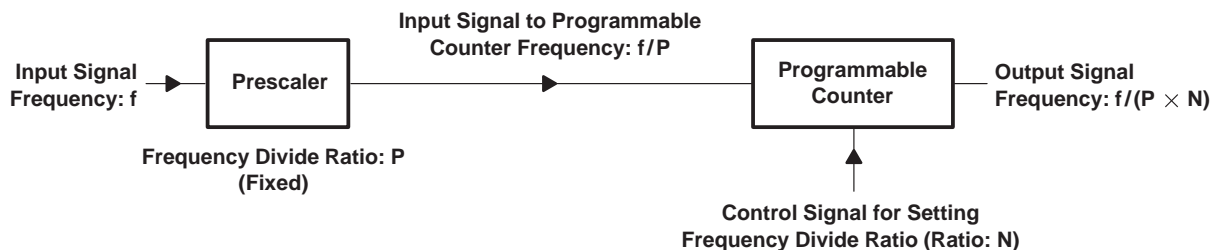


Figure 19. Prescaler Method

The prescaler frequency dividing ratio is fixed. As shown in Figure 19, if the prescaler frequency divide ratio is  $P$  and the programmable counter frequency dividing ratio is  $N$ , then the total frequency divide ratio becomes  $P \times N$ . As shown in Figure 20, if the frequency dividing ratios  $M$  and  $N$  of the programmable counters are changed, the VCO oscillating frequency is changed in steps of  $P/M$  times the phase-reference frequency. Thus the channel space (frequency resolution) becomes  $f_{REF} \times P/M$ . The PLL  $f_{REF}$  should be chosen to be  $M/P$  of the channel space. Thus, if  $f_{REF}$  is low, the loop-filter time parameters must be designed to be large with respect to  $f_{REF}$ ; however, the lock-up time can become too large for the application. Noise effects must be considered as well.

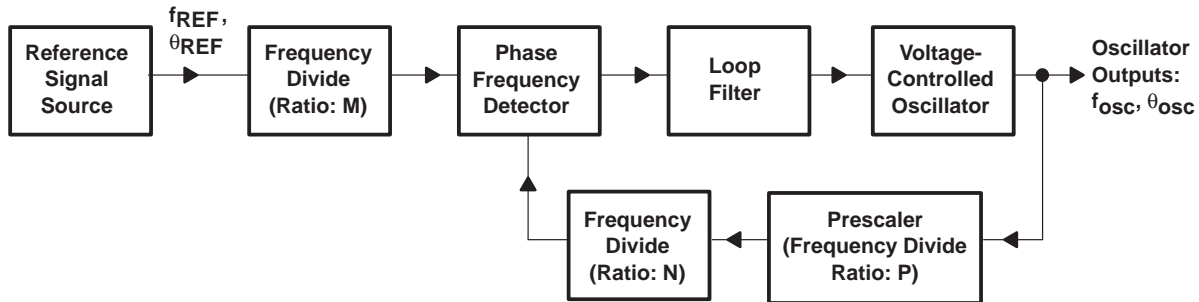


Figure 20. PLL Synthesizer Using Prescaler

### 2.8.2 Pulse Swallow Method (2s Modulus Prescaler Method)

When the channel space is equal to  $1/M$  of the reference frequency,  $f_{REF}$ , the technique is called the pulse swallow method. This method uses a prescaler whose frequency divide ratio can be changed by a control signal as shown in Figure 21.

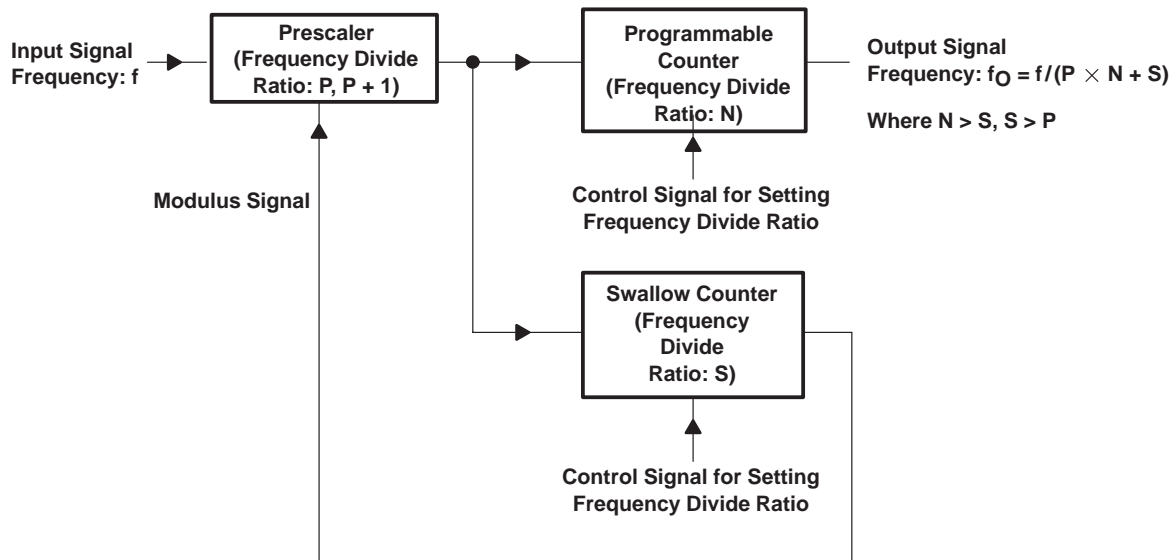


Figure 21. Pulse Swallow Method (2s Modulus Prescaler Method)

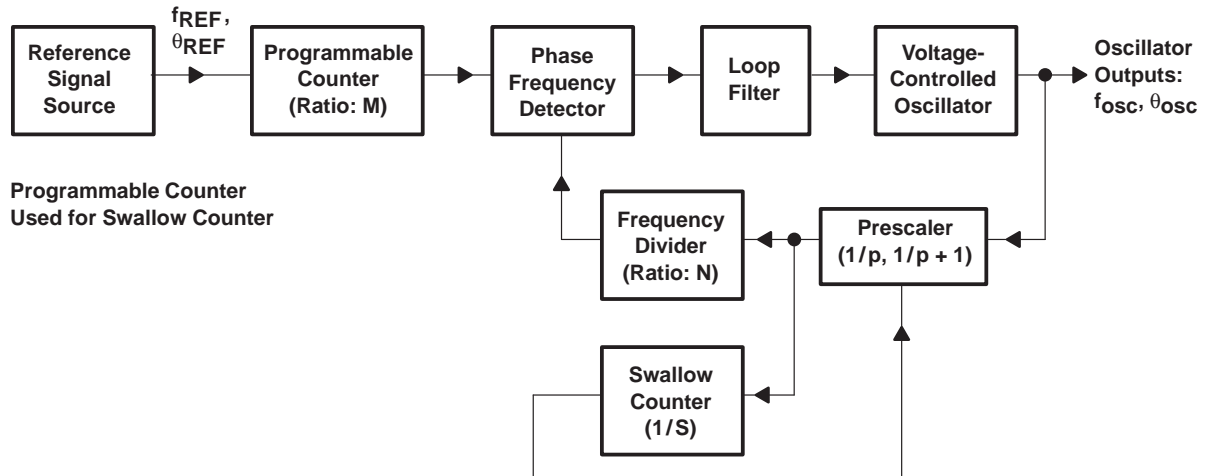
The prescaler frequency divide ratio is  $P$  or  $P+1$ . The counter consists of a programmable counter and a swallow counter which is used to control the prescaler. The frequency divide ratios are  $N$  and  $S$  respectively.

When the swallow counter is operating, the prescaler frequency divide ratio is  $P+1$ . The programmable counter and the swallow counter operate in parallel with the condition  $N > S$ . The swallow counter counts up to  $S$  and then generates a modulus signal to switch the prescaler. Then the prescaler's frequency divide ratio becomes  $P$ .

Thus, during the time period in which the swallow counter is dividing the frequency while counting up to  $S$  (time period  $S/N$ ), the total frequency divide ratio is  $(P+1) \times N$ . During the remaining time period,  $N-S$ , in which the programmable counter divides the frequency [time period  $(N-S)/N$ ], the total frequency divide ratio is  $P \times N$ . Now the output signal frequency can be expressed by the following equation:

$$f_o = f/(P \times N + S) \quad (38)$$

By examining the actual operation of the PLL shown in Figure 22 and equation 38,  $P$  is the coefficient for  $N$  but not for  $S$ . Thus, each time the value of  $S$  changes, the frequency only changes by  $f_{REF}/M$ . By using the pulse swallow method and a prescaler, a channel space of  $f_{REF}/M$  can be obtained.



**Figure 22. PLL Frequency Synthesizer Based on Pulse Swallow Method**

Many variations exist by combining frequency dividers. A specific frequency divider technique can be adopted according to the application.