

Homework 3: Due Thursday, April 1

Problem 1

In class we discussed a design technique for the row decoder that consisted of making subgroups of the address bits and using two levels of logic. The purpose of this technique was to reduce the total number of transistors and decrease the propagation delay. The total number of transistors depended on how the address bits were grouped. Your task is to...

- a) Derive a general equation that provides the total number of transistors needed for the decoder using standard CMOS logic. Assume you have N address bits for the row decoder, that each subgroup is K bits, and that there are an integer number of subgroups of the N address bits. For example, if you have a 16-bit address, you can only create groups of 2, 4, or 8 bits.
- b) Use this equation to find the optimal grouping of the address bits that produces the fewest number of transistors. In other words, find K as a function of N that produces the fewest number of transistors.
- c) Explain how you would estimate the worst case delay for the decoder given the optimal grouping you found in part b.

Problem 2

Given the charge pump that we studied in class, assume that the storage capacitor is 1pF, the pump capacitor is 0.1pF, $V_{dd}=3.3V$, $\beta_n=503 \mu A/V^2$, and $V_{tn}=0.5V$.

- (a) Calculate the clock frequency that is necessary to maintain less than a 10mV drop in V_{out} if a constant current of 1 μA is drawn from storage capacitor.
- (b) In steady-state at this clock frequency and for $I_{out}=1\mu A$, V_{out} will have a 10 mV ripple. Calculate the average steady-state value of V_{out} .