

ECE 551- VLSI Design and Testing I

Fall Quarter 2003

Instructor:	Mario Simoni
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Meeting Times:	Class: M, T, Th 11:45–12:35 Lab: F 10:50 – 1:30
Text:	John P. Uyemura. Introduction to VLSI Circuits and Systems. John Wiley & Sons, Inc. 2002.
Lab Tools:	Cadence Design Suite
Office Hours:	My office is D224. I have an open door policy. I will give you a schedule once my committee commitments have been assigned. I will arrive around 9am and disappear around 5:30pm in the evening.

Course Description

VLSI (very-large-scale integrated) circuit design involves using tens of millions of transistors to create integrated circuit systems. Such a task requires a breadth of knowledge, from the details surrounding complex digital (or analog) systems design to the details surrounding single transistor fabrication. Therefore, this class cannot be considered a purely analog or digital course. Although we may focus primarily on digital circuits and systems, we also must discuss the analog characteristics of transistors and how their physical structure affects the operation of circuits. These same insights can be applied to any purely analog or mixed-signal system. The range of topics that we will cover in this course are: (i) the relationships between mask layouts and circuit schematics, (ii) the relationship between device characteristics and CMOS circuit performance (including delays, noise margins, and power dissipation), (iii) the advantages and disadvantages of different logic styles (pass-gate, ratioed logic, dynamic), (iv) the analysis of worst case timing performance for any given circuit, (v) the effects of interconnect parasitics on system timing and the strategies to alleviate such problems and (vi) testing strategies of large systems.

Course Objectives

By the end of this course, I expect that you will be able to:

- Evaluate the effects of device characteristics on CMOS circuit performance
- Take device characteristics into consideration when analyzing or designing a CMOS logic circuit
- Create a mask layout of a circuit schematic
- Create a circuit schematic from a mask layout
- Sketch the physical structures from a mask layout
- Know how to design logic circuits using different logic styles (pass-gate, ratioed logic, dynamic logic)
- Analyze the worst case timing performance of digital circuits
- Analyze the impact of interconnect parasitics on system timing and know how to alleviate these problems.
- Apply the concepts of controllability and observability to circuit design to ease circuit testing.
- Design a moderately complex CMOS subsystem optimizing one or more of the objectives.
- Present your results in the format of a paper and a short presentation.

General Policies

Homework: Homework assignments will be assigned weekly. Late homework will only be accepted with a penalty, unless prior arrangements have been made. *I must be able to follow your work easily.* Your grade is not just a function of knowing the material, but also in being able to communicate it clearly. Sketches, schematics, and plots must be neat and labeled clearly. Layouts must be done using colored pencils or ink. Homework grading policy...

Completely Correct:	4
Minor Concept/Math Errors:	3
Serious Conceptual Errors:	2
Barely Attempted:	1
Not Attempted/Illegible:	0

Laboratory: The laboratory will be held in B200. Laboratory reports are due at the beginning of the next laboratory period. Unless prior arrangements are made, late lab reports will only be accepted with a penalty. The lab reports are meant to make you think about the material that you have been learning. I expect a reasonable amount of *thought and effort* to be placed into these reports.

Exams: There will be 1 midterm occurring in either the 4th or 5th week (I'll let you choose to avoid 3 exams on 1 day). There will also be a cumulative final.

Make-up Exams / Homework: Make-up exams will only be given in the case of a properly excused absence. Late or illegible homework will not be graded.

Grading Policy:	Homework:	15%
	Laboratory:	15%
	Midterm:	20%
	Final:	25%
	Project:	25%

Design Challenge: This year in the VLSI sequence you will be designing a single integrated-circuit modem. A modem is composed of both analog and digital components. In the Fall and Winter Quarters we will focus on each of these components individually and in the Spring Quarter we will integrate the components to create the complete system. In this class, VLSI I, you will design the digital component of the modem. You will work in groups of two or three and there will be a competition to decide which team has the design that will best integrate into the final system. In addition to using the winning-team's design in VLSI III, that team will receive a prize, the nature of which will be announced at the end of the quarter.

The digital component of a modem is basically a universal asynchronous receiver-transmitter (UART). The general idea of how UARTs work and the specifications for this particular project are available on the class web page. You will design the UART from scratch starting with state machine design and digital simulation and ending with fabrication-mask layout. Any team that wishes to do so may have their design fabricated and then test their design in VLSI III.

This project will be incredibly overwhelming if you wait until the last minute to get started. To help you keep your sanity, I will meet with each team three times during the quarter for brief (15 minutes maximum) design reviews to discuss your progress at each of the major steps of the design. Please feel free to meet with me about your design at any time throughout the quarter, these are just the official required meetings that will be graded. These reviews are meant to be low-key and very informal. However, your team is responsible for bringing the appropriate materials to the review that: 1) will enable me to understand what you are doing, 2) will help me to understand any problems you are having, and 3) will show that your design is working. It is **your team's responsibility** to email me and set up a meeting time at each of the following dates for each of the given reviews

Fri, Sept 19	Digital design and simulation of UART
Fri, Oct 24	Circuit design and simulation for each cell and resulting performance estimation
Fri, Nov 7	Mask layout design and floorplanning

A final project report and presentation will be due during our last lab meeting on **Friday, November 14**. For each of the three main design stages for which you had reviews, you should provide

- justification for your design decisions
- sufficient figures and descriptions of how your design works
- limited simulation results and effective descriptions of those results

The report should be between 6 and 12 pages and professional in appearance. The format is open, but you need to have at least the following major sections: Introduction, Digital Design, Circuit Design, Layout, and Conclusions. The introduction should show me that you know the basics of how a UART works and how it fits into the modem. The conclusions should state why you think your design is the best for integration into the system.

A 15 minute presentation of your project will be given at the end of the term. Please present only the major highlights. Do not go into detail on anything that has already been covered in class. The project grade will be broken down as follows:

Quality of Presentation	8%
Quality of Report	8%
Design Reviews and Other	9%