Lab 2: Layout of Your Inverter

Set up Other Partner's Account

- You should be using Cadence from the Partner's account you did not use in the first lab. To do this you will need to provide access to your designs from the first lab.
- Before you start Cadence, you need to copy three files from my /Users/faculty/simoni/Public/HTML/Classes/EC551/ directory
  - Copy the .cdsenv and .cshrc files to your $HOME directory
  - Copy the cds.lib file to your $HOME/cadence directory
  - Make sure that all partners have ALL of these files
- Type **souce .cshrc** to run the setup script (you only have to do this step this time)
- Start Cadence
- Add your design library to your Library Manager
  - In the Library Manager Window go to Edit->Library Path and a new window appears
  - Right-click on the first empty box in the Library column and choose Add Library...
  - Enter the information to choose the design directory in your partners account. For example /Users/class04/<partner1_username>/cadence/Labs
  - When you've finished go to File->Save and then File->Exit

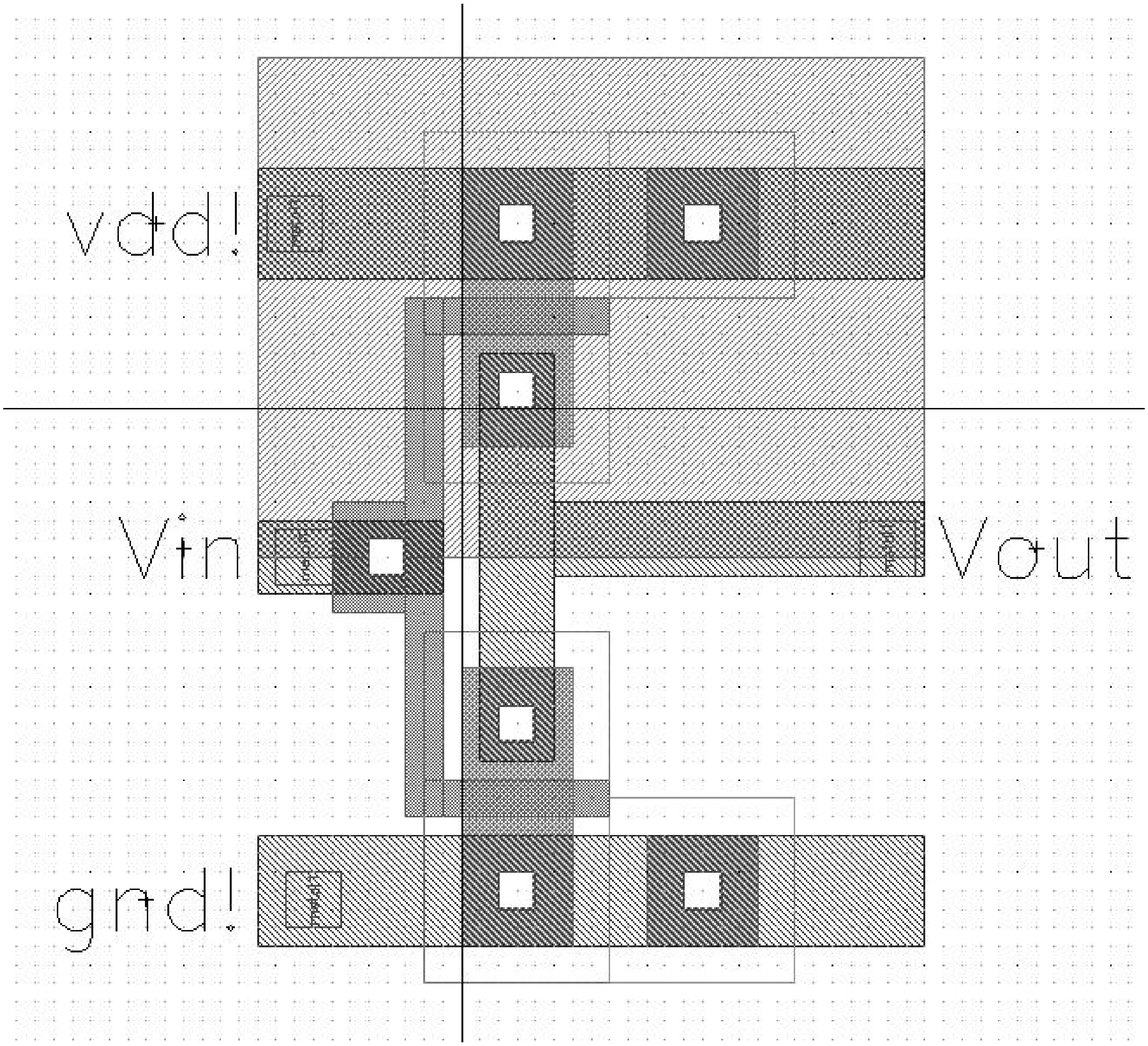
Create a Layout Cellview

- go to the Library Manager Window
- Create another cellview for the inverter
  - In the Design Manager window, select your *inverter* design.
  - Go to *File -> New->Cellview*
  - the cellname (*inverter*) and the library (*labs*) should be automatically entered
  - next to the Tool category select (*Virtuoso*) as the tool and the View Name (*layout*) will automatically appear. Conversely, you could enter the View Name (*layout*) and the tool would automatically be selected.
  - The layout tool should open
- Before beginning any layout, you should make sure that the grid is set correctly
  - Go to *options->display* (which can be evoked by the keystroke 'e')
  - If you successfully copied the .cdsenv file as mentioned above you should see
    - minor spacing - 0.3 um (How many lambda is this?)
    - major spacing - 1.5 um (How many lambda is this?)
    - xsnap - 0.15 um (How many lambda is this?)
    - ysnap - 0.15 um
    - in the Display Controls region "Pin Names" and "Instance Pins" should be selected

    NOTE: The snap spacing is different from the grid spacing. You can change the snap spacing to be the same as the grid spacing, but if you do, be sure to check this every time you reopen the layout or you will have a lot of headaches!! Also pay close attention to which design rules you can use if you change the snap spacing.

Begin drawing your inverter.

A diagram of the inverter is shown below. You may play with the editor yourself, or follow my directions below. Through my directions, I try to demonstrate many of the features of the program.



Accessing the Design Rules

- Before you start drawing polygons, open a web browser and go to the following URL: http://www.mosis.org/Technical/Designrules/scmos/scmos-main.html to access the design rules.
- Scroll through this web page and see if you can understand what everything means. If you need assistance please ask. The actual design rules are located under section: **3. CIF and GDS Layer Specification**
- Keep this web page available and reference it continually as you do your layout. Eventually you will begin to memorize some of the more common rules.

Draw a layer

- Click on the rectangle button on the left hand side to activate the draw mode.
- Choose the metal1 layer from the layer pallette (be sure you get the dg layer).
- Draw a rectangle 6λ wide that extends the length of your screen.
  - click in the background where you want one corner.
  - move your mouse. You should see a box demonstrating the size of the metal wire.
  - click where you want the opposite corner.
- hit the Esc key to get out of the draw mode

Copy a box

- enter the copy keystroke 'c'
  - In the pop-up window, notice the *snap mode* (orthogonal is really useful!) and the *change to layer* button.
- click on the wire (it should highlight)
- move the mouse and you will see a copy move with you (notice the effects of the snap mode)
- with your mouse in the background, you can use the arrow keys to scroll
- scroll once and place your wire at the bottom of the screen
- escape out of the copy mode

Resize your design

- enter the 'f' keystroke to fit your entire design on screen
- click in the background to deselect all elements (I'm sure there is a keystroke for this too).

Stretch your wires

- enter the keystroke for the stretch command ('s') (alternatively, click on the stretch button on the left hand side)
- box select (i.e. draw a box to select several items at once) both wires - one edge will be selected
- click on the highlighed edge, and move your mouse to the right
- click where you want the new edge to be
- note: stretch is a very useful command. Everything that is selected will be effected by this command. If some object is entirely contained in the box, it will be moved, not stretched. Anything that the box edge cuts will be stretched.

Make your pFet

- Create an active region that will become the source and drain of you FET. Make sure that it is 5λ wide and that one edge overlaps your top metal wire (your Vdd) (see picture).
- Add p-select surrounding the active, overlapping by 2λ on all sides.
- Add your poly gate, 2λ long, across your active region (see picture for orientation).
- Add your contact cuts (CC) on your drain and source regions.
- Add your substrate contact to the side of your FET.
  - Use a 6λx6λ box of active.
  - Surround the active with n-select. Make sure that your n-select and p-select abut to one another (to minimize area) but don't overlap (design rule violation).
  - Add your contact cut.
- Add your well. Be sure that it overlaps the active in the p-transistor by 6λ and the active in the well contact by 3λ.

Make your nFet

- Activate the copy command.
- Select the active, poly, and contact cuts. (Select multiple items by using the shift key and selecting)
- move these elements to the bottom rail.
- move your poly gate up one lambda.
- add your select (n-select around the transistor and p-select around the substrate contact).
- add a layer of poly to connect the two gates
- add a metal wire (4λ wide) to connect the drains of the two FETs
- make sure both drain and sources are connected to wires (i.e. make sure there is a contact cut!!)

Minimize your design

- The active of your nFET and pFET must be 12λ apart. However, there is no reason to make them further than this unless you have to (usually to route wires). Push your nFETs and pFETs as close together as possible.
  - activate the stretch command (make sure your snap mode is orthogonal)
  - box select all of you nFET stuff and your gnd wire
  - move everything so that the active in the nFET is within 6λ from your well edge
- Everything should have moved, except your poly wire connecting your gates and your metal wire connecting your source/drains - these should have stretched.

Add your pins

- It's MUCH easier to simulate if you have pin names. LVS is also easier. Make sure that any pin that you want to add a voltage source to later has a pin name.
- connect a 4λ wide metal wire to the poly - be sure that your poly overlaps the CC by 2λ on all sides, however your metal only has to overlap the CC by 1λ. Make sure that the metal wire goes to the edge of the cell.
- add a 4λ wide metal wire to the output that takes the output to the edge of the cell.
- to create a pin, select *Create-> Pin*
- in the pop-up window:
  - enter pin names (match your schematic names- *in out vdd! gnd!* - the ! indicates a global variable)
  - click on *display pin name*
  - I/O type - match your schematic pin type
  - pin type - match your layer (should be metal1)
  - move to window and pin box will appear
  - place pin by clicking and pin name will appear
  - move pin name where you want it and click to place

Save your layout

- I'd save as I went, since sliderule is not incredibly predictable
- click on the *save* button on the left hand side

Design Rule Check (DRC)

- click on Verify -> DRC -> OK
- the defaults are set up correctly now, but in larger designs you may want to DRC a small area (click on *checking limit -> by area*, box select the area you want to DRC)
- click OK - in the cds window, the number of errors should be displayed.

- The cds window should list the number of errors and the rule that has been violated. White boxes should show you where the error is located.
- If you don't have any errors, make one and see how the system notifies you.

Extract your layout (create a schematic netlist from the layout)

- click on Verify ->Extract.
- in the Extract window, click on the *set switches* button
- Choose "extract_parasitic_caps" and "keep_labels_in _extracted_view" (shift select to activate both)
- Click OK
- Look for any errors in the cds window.
- Open the extracted view (go to the library manager and double click on the extracted view of the inverter).
- You should see your layers with schematic symbols placed on top. If you do not see the schematic symbols, you need to tell the editor to see multiple levels. Use the "e" keystroke to bring up the display window. Enter the number of levels as 5.

Layout versus Schematic (LVS - compare your netlists)

- Go back to the inverter layout window.
- Click on Verify -> LVS
- In the LVS window, use the browse button under the schematic column (or type) to select your inverter schematic.
  - be sure you compare your schematic with your EXTRACTED view
- Hit OK and wait
  - you will see a window that says "LVS has succeeded". This just means it is done, not correct!!
- To see the results of the LVS, go back to the LVS window and press the *output* button.
- Look for the statement
  - "The net-lists match" or
  - "The net-lists failed to match"
- If the netlists don't match, you must find the error.
  - Click on the error display button
  - A new window will appear
  - Press the *Display -> First* button
  - The problem nodes will be highlighted on the schematic and the extracted view of the layout (note: you may need to open the schematic view)
  - Click on the *next* button to cycle through the problem nodes
- Fix your errors
  - if your problem is in the schematic, you MUST "check and save" again to update the netlist if yourproblem is in the layout, you MUST extract the layout again to update the netlist
- LVS again and fix problems until the netlists match.

Simulation of Layout

- Open your extracted view (if it is not already open)
- Click on Tools -> Analog Environment
- The simulator window should appear
- Your extracted view does not contain any sources or the load capacitance. The next steps are intended to add these elements to your netlist so you can simulate the layout.

- Create a stimulus file by going to Setup->Stimulus->Edit Analog...
  - give the file name invStim, choose the “text” option and click OK
  - A text window will appear in which you will enter the syntax for the stimulus file
  - Below is sample code to add a capacitor, a dc source for the power supply, and a pulse voltage source. You will need to create a file that follows this syntax, but use your node names. Note: 0 always refers to ground. The \! at the end of vdd represents a global node. **Make sure to set the text editor so that it does not wrap the text lines. In the text editor, go to Preferences->Wrap->No Wrap. Also be sure to include a carriage return after the last line.**

```
simulator lang=spectre

c0 (out 0) capacitor c=1e-12 m=1.0
v1 (in 0) vsource type=pulse dc=3.3 val0=0.0 val1=3.3 period=1e-6 delay=0.0 rise=1e-9
    fall=1e-9 width=0.5e-6
v0 (vdd\! 0) vsource type=dc dc=3.3
```

- In the simulator window, click on Setup->Environment
  - At the bottom of this form is a choice labled Include/Stimulus File Syntax
  - Make sure Spectre is selected and clik OK for the form
- In the simulator window, click on simulation->netlist->CreateRaw
- Then click on simulation->netlist->CreateFinal
  - anytime you make changes to your stimulus file you must first go to CreateRaw and then CreateFinal netlists to reload the new stimulus file.
  - look for the transistors (labeled m#). See if you can understand the connections. How are the gate, drain, source, and bulk nodes listed?
  - look for the models (listing all of the transistor parameters)
  - look for the sources that you added
- if you do not have each of the above components in your netlist, something went wrong. You must try again
- once you have a complete netlist, set up a transient analysis.
- Choose the outputs that you want to plot by selecting the nodes on the extracted view.
- Run the simulation and find the rise and fall time.
- Print out the rise and fall time.

Array your inverter to create a ring oscillator

- Go to the library manager and create a layout cellview for a new cell called ringOscillator
- In this new layout you want to create a ring oscillator with 36 inverters
- Before I sign off on your layout you must achieve the following goals
  - minimum area consumption
  - you can use only 8 wires on the top level of heirarchy to interconnect your inverters (this includes connecting all of your power and ground lines together)
- To instance your inverter layout use the button on the left hand side of the layout window
  - you may enter the cell name (inverter) or use the browse button
  - the Mosaic section of this form allows you to create arrays of the cell you are instancing (*hint*: making a 6x6 array at one time will not give you the minimum area)
  - the Delta X and Delta Y fields set the spacing between adjacent cells in the array
- To see the contents of the cells, pull up the *display options* window (keystroke ‘e’).
  - set the “display levels” from 0 to 5

- To change the spacing between cells in the array after they have been placed
  - Select the array
  - Click on the properties button on the left hand side of the screen
  - Adjust the Delta Y or Delta X fields until the cells abut next to one another
- You may need to adjust the placement of your input and output wires.
  - To do this, decend into the layout of the inverter (*Design -> Heirarchy -> Edit in Place*)
  - Choose which cell in the array you want to edit. It really doesn't matter since they're all the same.
  - You can now select and edit only the one cell in the array
  - Move the wire and notice how the change occurs in every cell in your array
  - Return to the upper level (*Design -> Heirarchy -> return*)
- When you think you have met the design goals, ask me to check off your layout
- We will perform LVS and DRC of this layout in future labs

CONGRATULATIONS!!! You just designed your first layout with a total of 72 transistors!

Informal Lab Report

Include the following sheet with the check points signed off. Be sure to include printouts of the layouts and the DC and transient characteristics of the inverter schematic.

Your Names: ____

Inverter Layout check ____________________________________

DRC check ____________________________________

LVS check ____________________________________

Ring Oscillator Layout check ____________________________________

Inverter Layout Simulation

Rise/Fall time: t_{rise} ______________________ t_{fall} ___________________________

Questions and Calculations for Informal Lab Report

You may use this sheet or attach additional pieces of paper to answer the questions.

1. Print out your inverter layout and label the pFET, the nFET, and the bulk connections.

2. When creating the inverter, why did we pull the input and output wires to the edge of the cell?

3. What is the advantage of editing your layout in its place in the system versus in isolation in a separate window?

4. Compare the rise and fall time of your schematic to your layout. Discuss the differences and why you believe these differences exist.

5. What is the purpose of LVS?

6. If you have simulated your schematic, why do you also have to simulate your layout?