

Lab 1: Schematic Entry and Simulation

Log into sliderule:

- Start XWin32. Go to Start->Programs->XWin32 5.3 -> XWin32
 - Hit Cancel when the window pops up and you will see a little blue X appear in the lower-right corner of your screen
- Start SecureCRT
 - Once you set up the ssh2 session you need to enable X11 packet forwarding
 - In the SecureCRT window menu go to Options->Session Options...->Connection->Port Forwarding->X11
 - Check the box that says Forward X11 Packets
 - Then you have to quit and restart SecureCRT
- Login to sliderule

Set up Cadence directory:

- Cadence needs a special directory to use as a home base for all of the files you will create.
- Whenever you start Cadence it will automatically start from this directory.
- Create this directory as a sub-directory of your HOME directory by typing:
mkdir \$HOME/cadence
(note: unix IS case sensitive, make sure you follow the cases EXACTLY as written here!!)
- Enable your lab partner to have access to your design directory, at the command prompt type:
fs sa \$HOME/cadence <your lab partner's username> rdliwka

Common Unix Commands

- **mkdir** - make directory
- **ls** - list files
- **cd *directory*** - change directory
- **cd ..** - go up one directory level
- **cd ~** - go to home directory
- **rm *filename*** - remove file
- **rmdir *directory*** - remove directory

Run Cadence design tool suite:

- Copy the following setup file to your home directory by typing:
cp /Users/faculty/simoni/Public/HTML/Classes/EC551/.cshrc \$HOME/.cshrc
- Run this setup file by typing: **source .cshrc**
 - Note: You only have to run this setup script this time. In the future, this script will be run automatically whenever you login
- To start Cadence type: **icfb**
Several windows will appear.
- Disable the “What’s New” window by going to that window’s Edit menu. Then close this window.
- The “icfb - log” window will be your window to all error messages and all operations that are occurring in your program. Make sure you can see it at all times.

Set up a Library

Cadence will create MANY files for every design that you create. You can have a single *cell* (e.g. inverter, NOR gate, Adder) that has several *cellviews* (schematic, symbol, layout) The software ties each of these cellviews together to simplify debugging. It is usually best to keep all of the cells for a large designs under a single library name (which also corresponds to a directory). Every cell in a given library should use the same *technology* (e.g. Scalable Cmos Nwell Electrode (SCNE) 0.5u) which provides all of your models for simulation and layout.

- go to *Library Manager* window
This window will let you access all of your files, move files (DO NOT move them using unix commands, or you will lose something), delete files, and add new libraries.
- to create a new library, go to *File -> New -> Library*
 - enter *Labs* for the Library name and leave the path blank
 - At the bottom of the Create Library window you have a choice of three buttons. Choose “Attach to existing tech library-->”
 - When you choose this option, a selection bar will appear to the right. Scroll down to select AMI 0.6u C5N (3M, 2P, high-res)
 - Click on OK at the top of the Create Library window

Create an Inverter Schematic

Create an inverter with transistor values of $W=0.9\mu$ and the $L=0.6\mu$

- Create a new cellview
In the *Library Manager* window, select the *Labs* library.
Go to *File -> New -> Cellview*
Enter the cellname (*inverter*)
Select the tool which will select the cellview (*Composer - Schematic*)
The schematic tool should open
- Instance your devices.
Click on the *Instance* button on the left-hand side of the editor (you can also type “i”)
A separate window should appear
Choose the *N_Transistors* set
Choose the *nmos4* cell
Place the nFET by clicking on the canvas.
Get a *pmos4* from *P_Transistors*, and *vdd* and *gnd* from *Supply_Nets* .
Hit the escape key to get out of that function. (This will work for all functions)
- Move your devices if you need to. (go to Edit -> Move, click on the device once to pick it up and a second time to drop it.)
- Wire the circuit elements together
Click on the *wire* button on the left-hand side. (make sure you get the NARROW wire, not the wide wire (which is for bus connections)).
Click a port to begin wiring, click another port or wire to connect two elements together.
Double click if you want to end the wire unattached.
NOTE: you can also add wires simply by clicking on a port and dragging the mouse
- Once the FETs are properly placed, choose each transistor and click on the *properties* button to the left-hand side to see the transistor properties. You may also modify a group of elements

of the same type by selecting the *Apply to: all selected* button at the top of the properties window.

- In the properties window, set up your transistor model
width: 0.9u
length: 0.6u
- Add an input and an output pin to your inverter.
Use the *add pin* button on the left-hand side.
Enter all pin names separated by spaces (*in out*).
As you place the pins in the schematic, select the pin direction (i.e. input, output, bidirectional).
Using bidirectional ports for everything will simplify hierarchical design later.
- Save your file.
Click on the *check and save* button on the left-hand side.
This also creates a netlist, which will be needed later when we compare the Layout versus the schematic (LVS)).

Create an Inverter Symbol

Turn the inverter schematic into a symbol.

- Go to *Design -> CreateCellview -> from cellview* (all defaults should be correct)
- Click OK
- In the Symbol Generation window, specify where you would like your pins to go.
- Click OK
- A box will appear with your symbol.
- You can delete the green box and change it to a normal inverter symbol, but be sure to not delete your pins (the tiny solid-red boxes), the part name, the instance name, or the hollow red box that goes around everything.
- Save your symbol (menu on left-hand side)
- Close the window (*window -> close*)

Simulate the Inverter (DC and transient characteristics)

- Create a new cell called *InverterTest*.
- Instantiate your new inverter symbol.
- Instantiate a DC power supply *Voltage Sources -> vdc*
- Instantiate a Vdd and Gnd net and connect the DC supply to these nets
- Set the DC supply to 5V through its properties window
- Add a pulsing voltage source (*Voltage Sources->vpulse*) to the input and a 1pF capacitor (*RLC->cap*) to the output. You can use this source for both the DC and transient analysis.
For transient analysis: Make the rise and fall time of the pulse = 1ns, the pulse width=1us, period=2us, and delay time=0.
For DC analysis: choose this voltage source when prompted by the *Analysis->Choose->DC* window
- Start the simulator (*Tools -> Analog Environment*) from the schematic window.
- In the simulator window:
Choose a simulator (*setup->simulator->spectreS*)
Set up your analysis type (*Analysis->Choose*)
Select your outputs (*Outputs->to be plotted->select on schematic*).

Click on wires to get a voltage

Click on ports to get a current (positive current is assumed to go into the pin)

- Run the transient analysis so that you can see one full period of the pulsing input
- Run the DC analysis from Gnd (0V) to Vdd (5V)
- Click on the green button to run the simulation.
- A window should automatically appear with the curves drawn.
- You can add cursors to the window to display curve data more accurately.

Modify the Output Capacitance and Resimulate

- Double the capacitance on the output of the inverter and note the result on the simulation.

Informal Lab Report

Include the following sheet with the check points signed off by me. Be sure to include printouts of the schematic, both DC characteristics, and both transient characteristics in the final lab report. Also, please include answers to the following questions. Lab report is due at the BEGINNING of the next lab session. You may come into the lab during the week if you need to finish any portion of the lab as long as you are not taking away a computer needed for another scheduled course.

Name: _____

Lab Partner: _____

Inverter Schematic check _____

Inverter Symbol check _____

Inverter Simulation

DC characteristics check _____

Inverter Threshold: V_{thresh} _____

Transient characteristics check _____

Rise/Fall time: t_{rise} _____ t_{fall} _____

Modified Inverter Characteristics

DC characteristics check _____

Inverter Threshold: V_{thresh} _____

Transient characteristics check _____

Rise/Fall time: t_{rise} _____ t_{fall} _____

Questions and Calculations for Informal Lab Report

You may use this sheet or attach additional pieces of paper to answer the questions. Please attach an additional sheet of paper for the calculations. If you do the calculations in Maple, be sure to attach the Maple code showing the calculations and highlighting the answers.

1. Why is it important that we create symbols for our schematics?
2. Why did we add the capacitor to another “test” schematic rather than adding it directly to the inverter schematic?
3. Why is it so critical to be able to easily move through different levels of the hierarchy?
4. Please describe the effects of the capacitor values on the transient inverter simulations.
5. Printout of the DC characteristics. Why is the switching region so wide?
6. Given the DC characteristics, how would you define a logic 1 and a logic 0 in terms of voltages and why would you pick those values?
7. Measure the rise and fall time of the inverter. Given these values, what would you say is the time delay of the gate and why?
8. Printout of the transient characteristics showing how you measured the rise and fall time.
9. Discuss why you think the rise time is different from the fall time.