

Homework 2: Due Monday, Sept 29

Problem1 (Section 6.1)

Do problem 6.1 in the textbook.

Problem 2 (Sections 6.2.2, 6.4)

A pFET has a gate oxide with a thickness of $t_{ox}=120 \text{ \AA}$. The n-type bulk region is doped with phosphorous at a density of $N_d=8 \times 10^{14}$. It is given that $|V_{T0p}| = 0.55 \text{ V}$ and $(W/L)=10$.

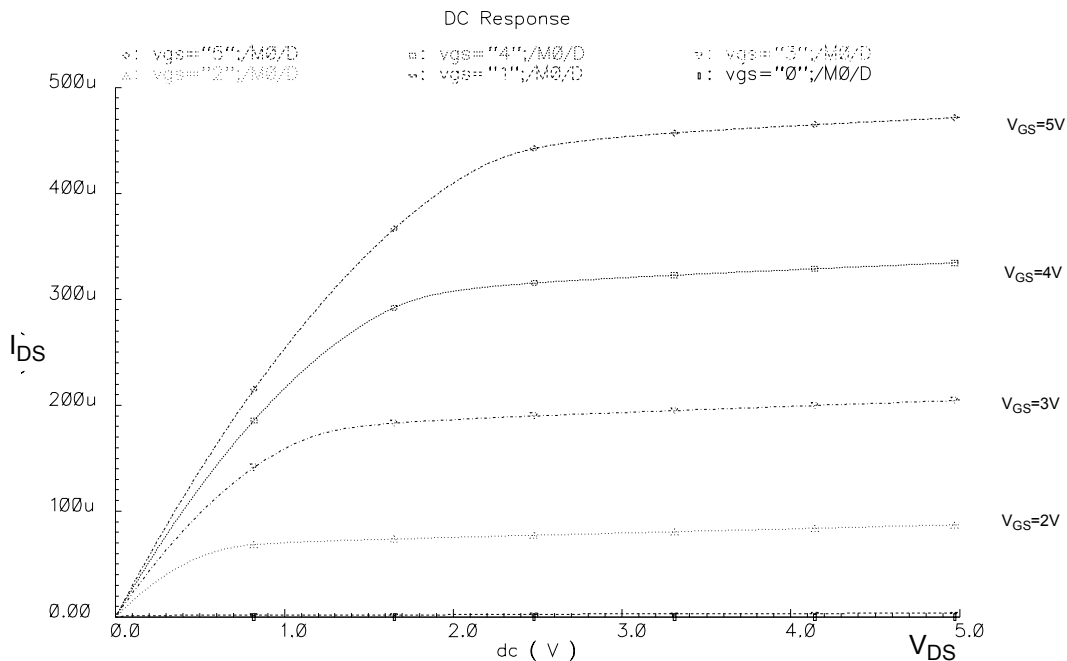
(a) Calculate the body bias coefficient γ_p .

(b) What is the device threshold voltage if a body bias voltage of $V_{BSp}=2\text{V}$ is applied?

(c) The hole mobility is $220 \text{ cm}^2/\text{V}\cdot\text{s}$. Calculate the drain current with bias voltages of $V_{SGp}=3\text{V}$, $V_{DSp}=3\text{V}$, $V_{BSp}=3\text{V}$ applied to this device.

Problem 3 (Section 6.2, Notes)

I have shown below the output current of an n-FET for different values of V_{DS} and V_{GS} . On this graph, label the different regions of operation for the transistor (linear region, saturation region, etc). Explain in your own words what is happening with the channel to create the observed response in each of these regions.



Problem 4 (Section 6.2.2, Notes)

Short Answer:

- (a) Give a brief description in your own words for the causes of channel-length modulation. Why do we ignore channel-length modulation when doing digital design?
- (b) Give a brief description in your own words for the causes of the body effect. What is one consequence of the body effect on digital design?
- (c) Why must the value of V_{DD} decrease as the process size decreases?

Problem 5 (Section 6.2)

Do problem 6.3 in the textbook.