

Homework 1: Due Thursday, September 18

Problem 1

Design a CMOS logic gate to implement the following functions:

a) $C_o = (X\bar{Y} + \bar{X}Y)C + XY$

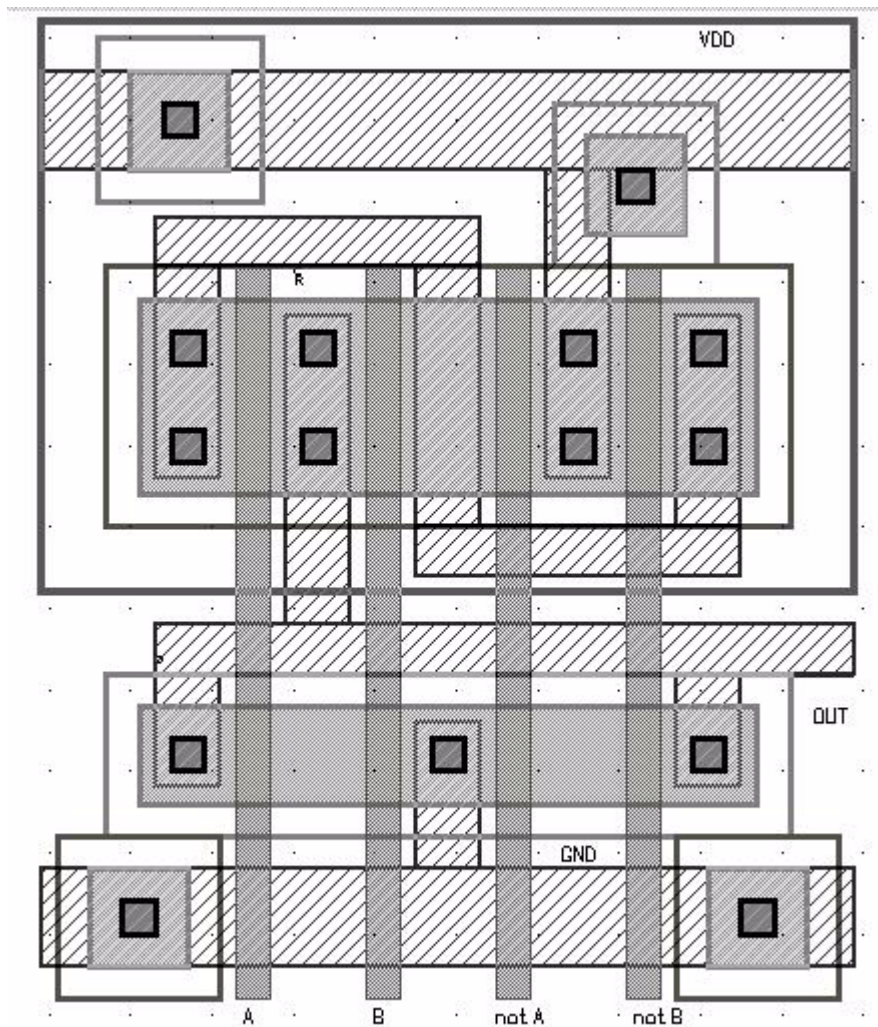
b) $Y = \overline{(A\bar{C} + ABC)\bar{D}}$

Problem 2

Design a 4:1 multiplexor using pass-FET logic. You must use the minimum number of transistors to get full credit.

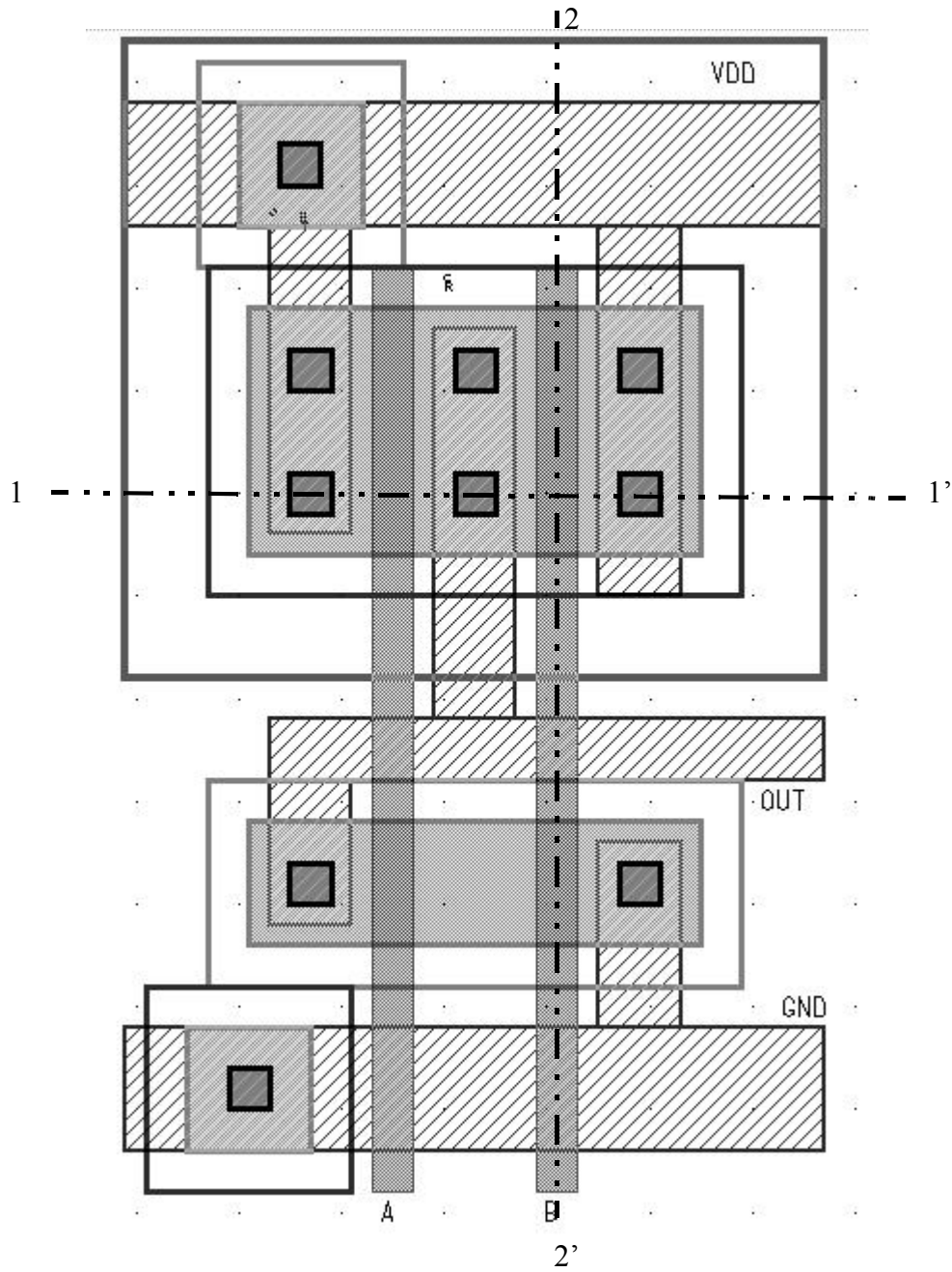
Problem 3

Draw the corresponding circuit diagram of the following layout.



Problem 4

Sketch the cross-sections 1-1' and 2-2' indicated in the mask view of the CMOS NAND gate shown below. Be sure to label your diffusion type clearly.



Problem 5:

The group of transistors below implements the function

$$F = \overline{\overline{AB} + \overline{AB}}$$

Using colored pencils, draw the stick diagram for the following circuit using a flipped cell layout topology for all devices that are connected to the inputs. Assume you are using an n-Well process with 1 Poly and 2 Metal layers. There should be common Vdd and Gnd lines. Make your design as compact as possible.

