

EC551

Fall 2003 Exam I

Name: _____

This is a take-home exam, and you may use your book, notes, homework, and computer, but not your friends. If you have any questions, please see me. Good Luck!!

For **ALL** problems assume the following parameters for your FETs...

nFET

$$k'_n = 146 \mu\text{A}/\text{V}^2, \gamma_n = 0.0639 \text{ V}^{1/2}, 2|\phi_F| = 0.568 \text{ V}, V_{Tn0} = 0.7 \text{ V}, C_j = 0.5 \text{ fF}/\mu\text{m}^2, C_{jsw} = 0.25 \text{ fF}/\mu\text{m}^2$$

pFET

$$k'_p = 52 \mu\text{A}/\text{V}^2, \gamma_p = 0.226 \text{ V}^{1/2}, 2|\phi_F| = 0.7 \text{ V}, V_{Tp0} = -0.7 \text{ V}, C_j = 0.6 \text{ fF}/\mu\text{m}^2, C_{jsw} = 0.3 \text{ fF}/\mu\text{m}^2$$

Assume that All FETs have a **drawn** $L = 0.6 \mu\text{m}$, $V_{dd} = 5 \text{ V}$, $C_{ox} = 1 \text{ fF}/\mu\text{m}^2$, and a gate overlap of the drain/source regions of $L_0 = 0.1 \mu\text{m}$.

Grade:

Problem 1: (30 pts.) _____

Problem 2: (20 pts.) _____

Problem 3: (20 pts.) _____

Problem 4: (30 pts.) _____

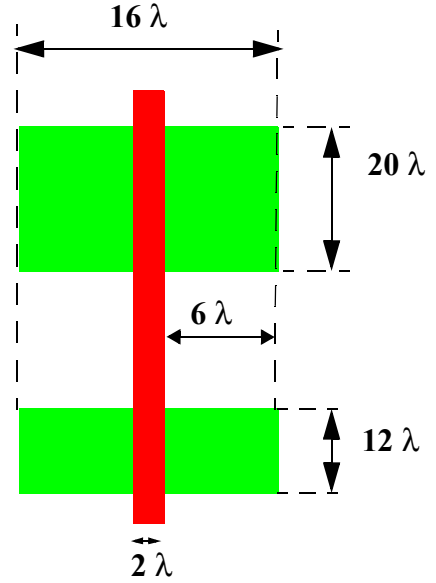
Total: (100 pts.) _____



Problem 1: FET Capacitance

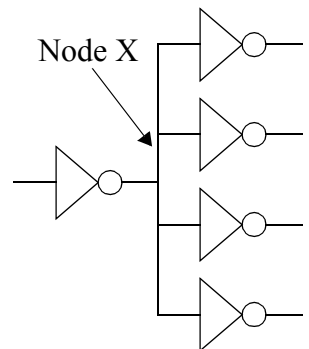
Assume you have a CMOS inverter with $(W/L)_n=6$ and $(W/L)_p=10$. The ACTIVE and POLY layers for the inverter are shown below. Note drawing is in units of lambda.

(a) Find the gate capacitances C_{Gn} and C_{Gp}



(b) Find the D/S Capacitances C_{Dn} , C_{Sn} , C_{Dp} , and C_{Sp}

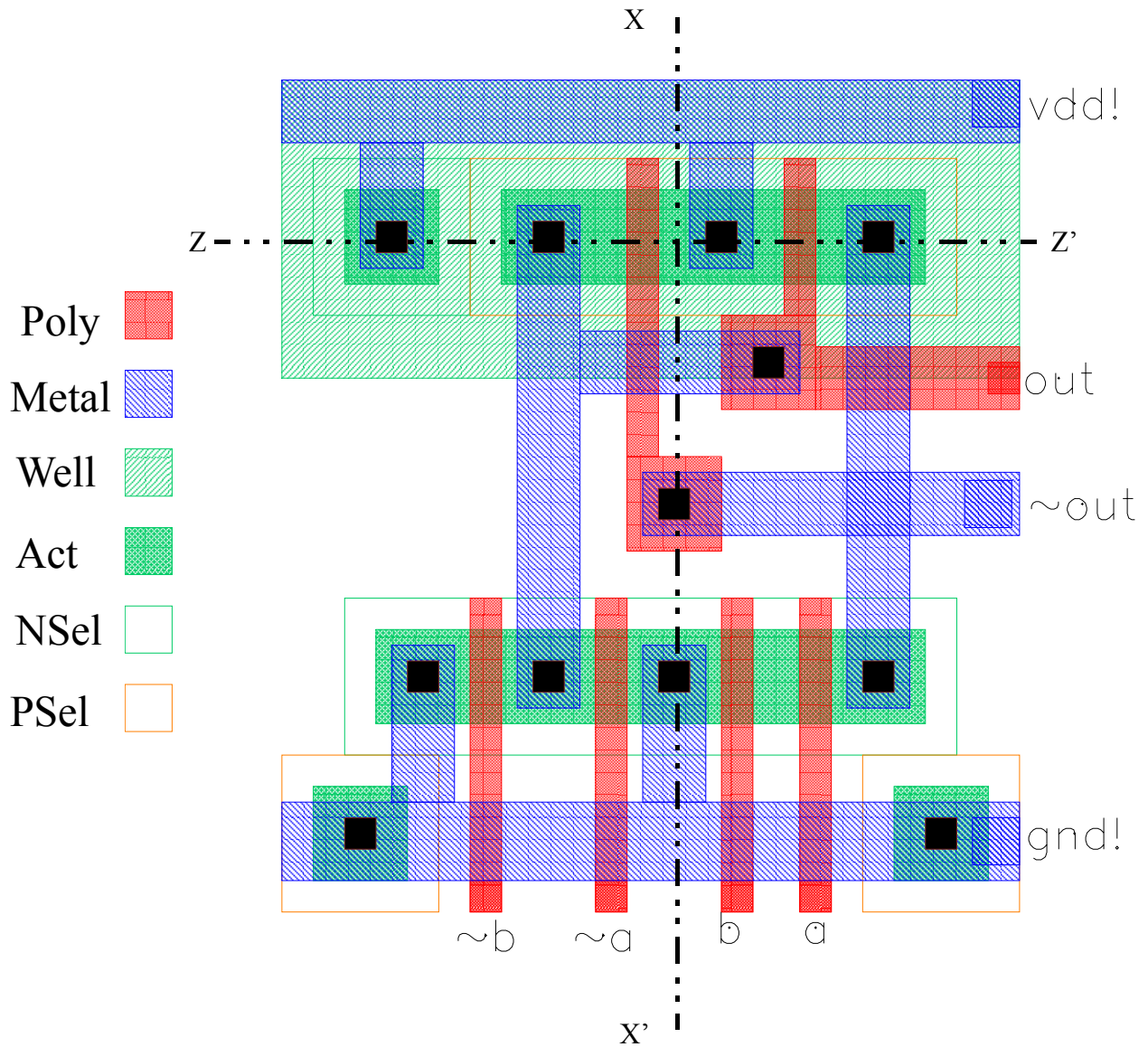
(c) This inverter is used in the circuit shown to the right. Find the total parasitic capacitance at Node X.



Problem 2: Layout

Given the mask layout shown below, answer the following two questions. The next page is left blank for you to solve this question.

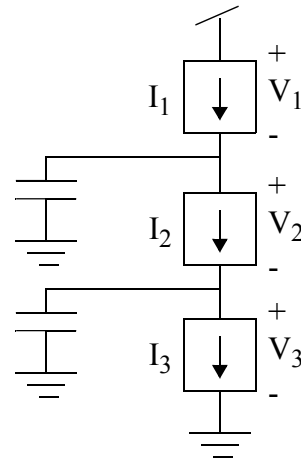
- (a) Draw the corresponding circuit diagram of the layout. (20 pts)
- (b) Sketch the cross-section X-X' and Z-Z'. (10 pts each)



Problem 3:

(a) The circuit to the right contains three non-ideal DC current sources (hence the square symbol instead of round) connected in series with parasitic capacitance at each internal node. The initial conditions and the constraints on the current sources are given below.

Current-Source Constraint: Each current source generates a nominal current that is set by an external input. As the voltage across the current source increases the current generated increases from the nominal value. As the voltage across the current source decreases the current generated decreases from its nominal value. At $V_x=0$ V the generated current is 0 A.



Initial Conditions: $I_1 > I_2 > I_3$, all voltages are positive and are such that each current source is sourcing its nominal value.

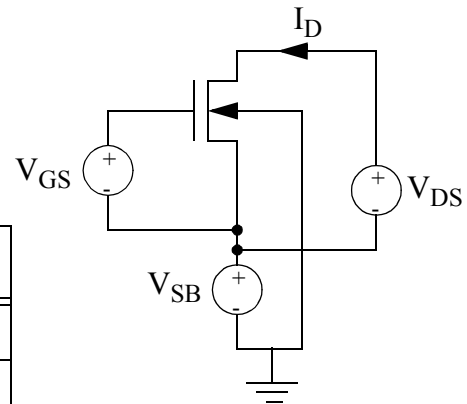
Determine the resulting steady-state current through the chain of non-ideal sources. Explain your answer in words and/or mathematical calculations.

(b) Explain in detail how this circuit relates to MOSFETs and logic gate design.

Problem 4: (25 pts)

A set of I-V measurements for an nMOS transistor at room temperature is shown in the table below. The parameters for this device are different from those listed on the cover page. Some of them are: $W/L=1.0$, $t_{ox}=345$ angstroms, and $|2\phi_F|=0.64$ V.

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μ A)
4	4	0.0	256
5	5	0.0	441
4	4	2.6	144
5	5	2.6	256



(a) Use this data to find the threshold voltage of the transistor V_{T0n} .

(b) Use this data to find the electron mobility μ_n .

(c) Use this data to find the body effect coefficient, γ_n .