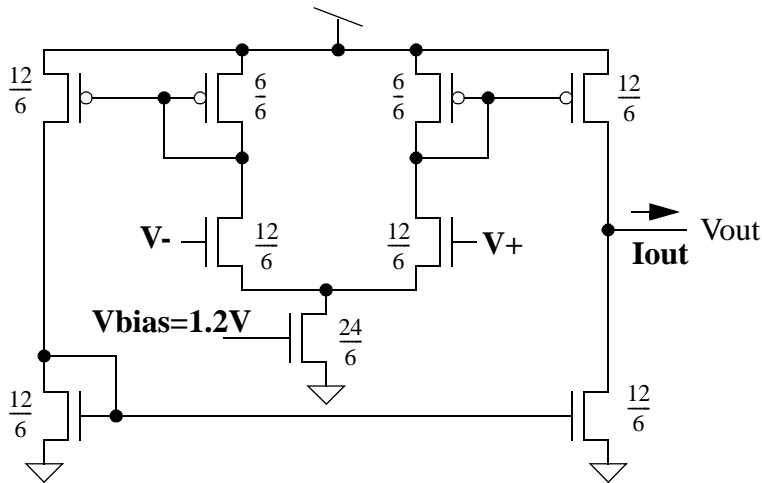


Optional Homework 6: Due Thursday, Feb, 20th

Problem 1

(a) Modify the following circuit so that it is a hysteretic comparator that compensates for 200mV of noise peak to peak. Assume that $K_n=20\mu\text{A}/\text{V}^2$, $K_p=18\mu\text{A}/\text{V}^2$, $V_{tn}=0.7\text{V}$, $V_{tp}=-0.9\text{V}$, $\lambda_n=0.1$ and $\lambda_p=0.2$.



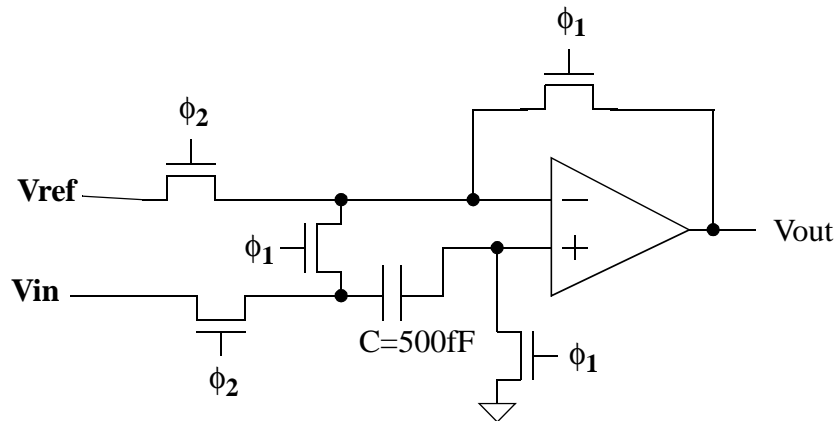
(b) Explain how positive feedback in any comparator (i) produces hysteresis and (ii) prevents false firing.

(c) Explain in your own words how the positive feedback operates in the comparator you designed in part (a).

Problem 2

Explain how the following autozeroing amplifier eliminates offset. Describe what happens in each phase of the clock. Assuming that 50fA leak through the switches, what is the minimum clock speed allowed that guarantees the voltage only changes by 1%? Assume that ϕ_1 and ϕ_2

are 2-phase nonoverlapping clocks. Both clocks are high for equal periods of time and both clocks are off for 20% of the clock cycle.



Problem 3

Find the expression for the input noise of the 2-stage comparator described in class. Include $1/f$ and the thermal noise in the channel. (Note: the noise in the first stage is scaled by the gain of the second stage). Once this expression has been found, how can we use layout techniques to minimize the noise?