

Summary for the Substrate Noise Hardware Lab

Summary of the Chips

Our analog and mixed-signal VLSI course uses two hardware labs. The substrate noise lab demonstrates the effects placing analog and digital circuits side-by-side on a single substrate. The students experiment with circuits that are laid-out with and without guard rings and shield wires to observe the effects of these layout techniques on the substrate noise. Additionally, the students experiment with two different versions of a transconductance amplifier (TA). The chip has been fabricated using the AMI 0.6 μm process and are contained in the area of a Tiny Chip (1500 μm X1500 μm).

Comparison of Two Trans Amps: The first set of experiments uses two different layouts of a transconductance amplifier and compares their output characteristics. The first trans amp is a simple 5-transistor trans amp, shown in schematic and layout form in Figure 1. The extra transistors on the outside of the pFET mirror are there to guarantee sufficient doping of the well under the mirror transistors. The second trans amp, shown in schematic and layout form in Figure 2, uses common centroid input FETs to reduce mismatch among the input FETs, and a cascode bias transistor. The cascode bias reduces the effects of channel length modulation, thereby producing a positive and negative saturation current that are closer to one another, at the consequence of limiting the common mode input range. The output characteristics of these two amplifiers are measured and compared by the students.

Simple Trans Amp (TA₁)

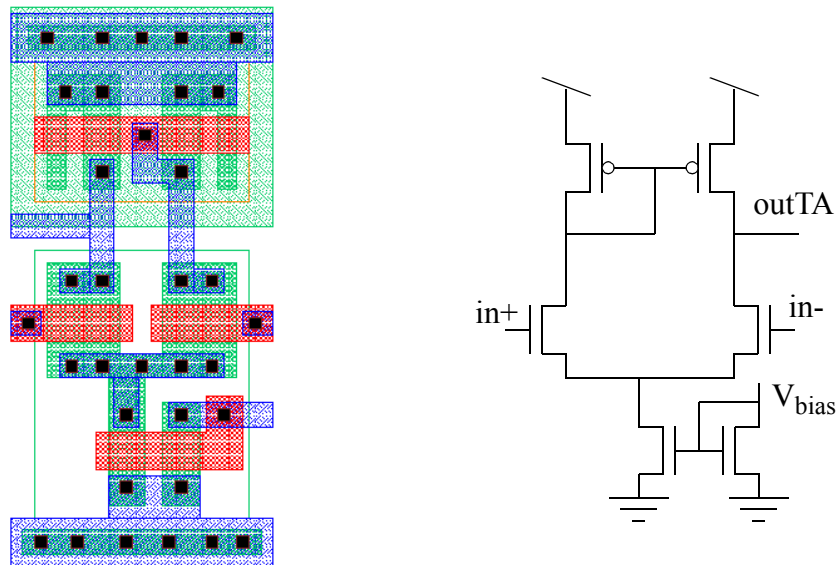


Figure 1: Layout and schematic of a simple 5-transistor transconductance amplifier.

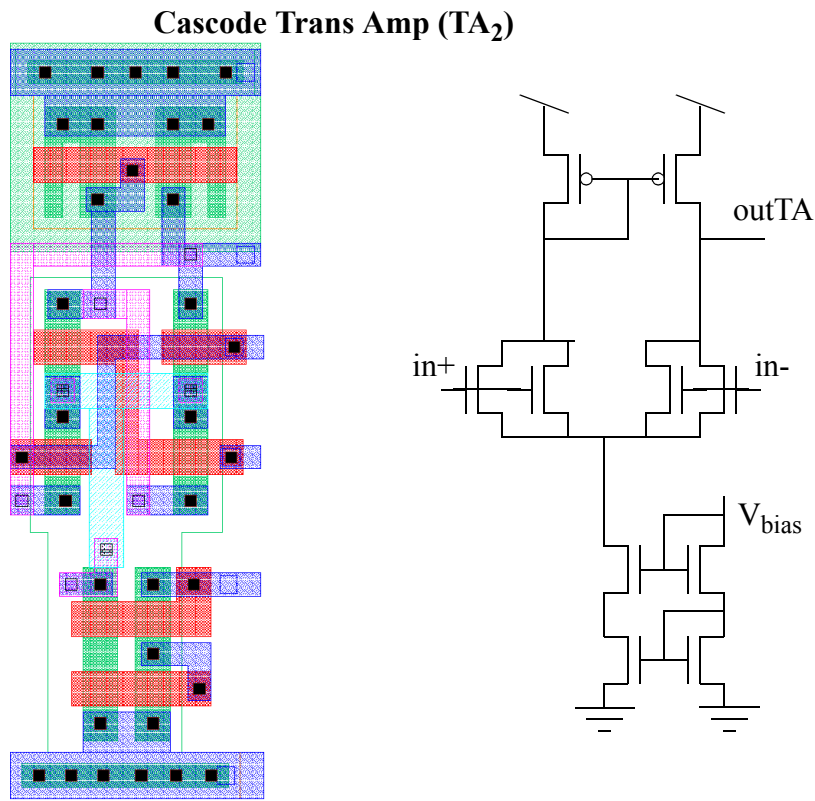


Figure 2: Layout and schematic of a transconductance amplifier using common centroid input transistors and a bias connected in the cascode configuration.

Effects of Substrate Noise: Four instantiations of TA₂ are placed on opposite corners of the chip. Beside each of these instantiations is a large array of digital inverters that may be controlled via a function generator or connected in a ring counter configuration. The digital inverters generate a significant amount of substrate noise. One TA (upper right corner of the chip) does not make any attempt to shield the digital noise from the analog circuit and contains a common power and ground wire between the digital and analog circuit. The second TA (lower right corner of the chip) shields the analog and digital circuits from one another using a guard ring and a ground wire shield (shown in Figure 3). However, this circuit also shares a common power and ground wire. The third circuit (upper left corner of the chip) does not shield the analog and digital circuits, but uses independent rails for the analog and digital circuit. The fourth circuit (lower left corner of the chip - shown in Figure 3) uses independent rails and separates the analog and digital circuits using a guard ring and a ground wire shield. The students can observe the interference of the digital circuit on the analog circuit by monitoring the output of the trans amp. While the effects of the guard ring and shielding on the behavior of the trans amp are evident, the effects of common versus shared rails are not evident. In fact, the shared rails do not demonstrate any interference with the trans amp behavior. We believe this lack of interference is because the inverter array fails to create a sufficient current to cause an IR drop across the rails. Because all inverters are not changing states at the same time, the current draw for the inverter array is fairly constant, and therefore it does not interfere with the operation of the trans amp. As a consequence, we are investigating a new ver-

sion of this chip so that these effects may also be measured by the students in future revisions of the lab (see Future Revisions section below). Because the current version of the chip does not exhibit noise with the shared rails, the lab only asks the students to experiment with two of the four circuits, demonstrating the effects of the guard ring and shield. The lab will be modified in the future when the new chip design is verified.

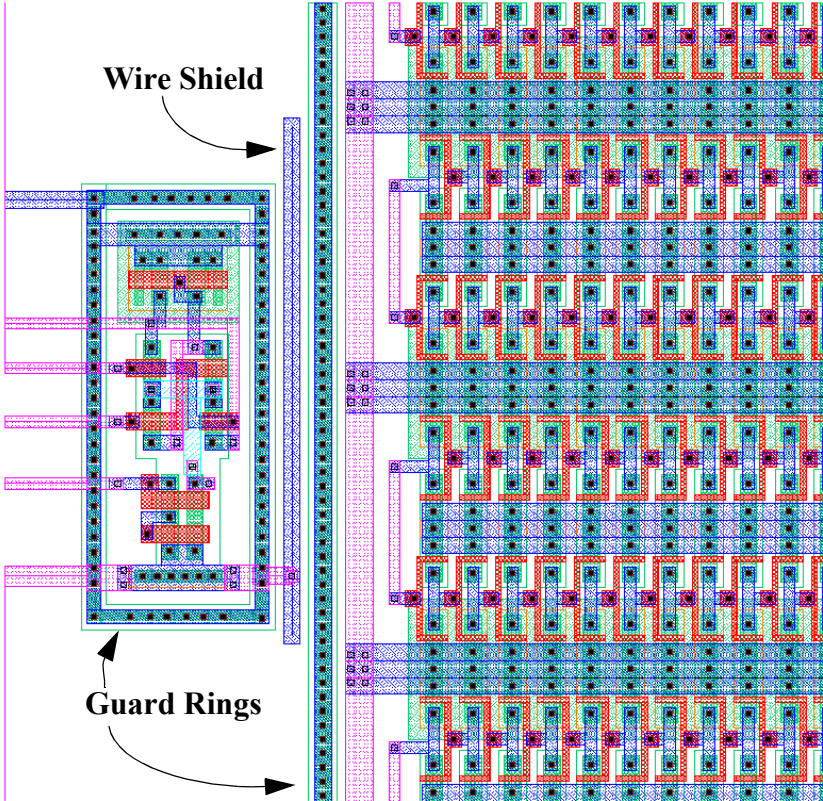


Figure 3: Layout of trans amp beside inverter array showing guard ring and ground wire shield.

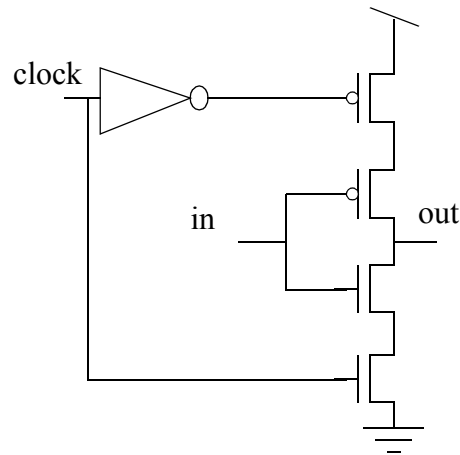


Figure 4: Schematic of the C²MOS latches used to replace the inverter array in the new version of the chip.

Future Revisions: In the next version of the chip, we have modified the inverter ring so that the effects of digital power and ground bounce may be observed on the trans amp. We have replaced the inverter chain with an array of clocked CMOS (C²MOS) latches, shown in schematic form in Figure 4. Each latch has an inverter in the cell, which will find the complement of the clock. Therefore, each clock pulse will draw a significant amount of current, causing an IR drop across the power lines. For the circuits that share a common power line between the analog and digital circuits, the power bounce will effect the behavior of the trans amp, demonstrating the need for analog and digital circuits to have independent rails that are connected external to the chip. The new circuit has been designed and submitted for fabrication; however we do not have confirmed test results to date. The new cif is available by request.