Summary and Expected Results for the Mirrors Hardware Lab

Summary of the Lab and Expected Results

Prelab

The students begin with a prelab, where they examine the layout of the different circuit blocks. The students hypothesize which subcircuit will provide the best performance in each circuit block. They are also asked to explain their ranking to encourage the students to think about the effects of layout on matching. Experimental results may not exactly match the students' predictions, but the intent is for the students to begin thinking about how layout variation, process parameters, and process variation will effect circuit performance.

First, the students are asked to look at the *transistor mismatch block*, shown in Figure 1, and make three predictions: (i) predict the relative currents between the two nFETs, where W/L = (9*W)/(9*L), (ii) predict the relative currents between the pFET and nFET of equal W/L ratios, and (iii) predict the relative channel length modulation for each of the FETs.

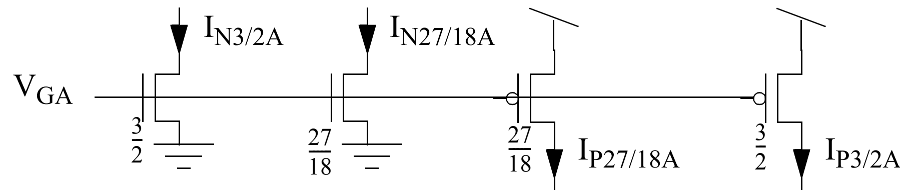
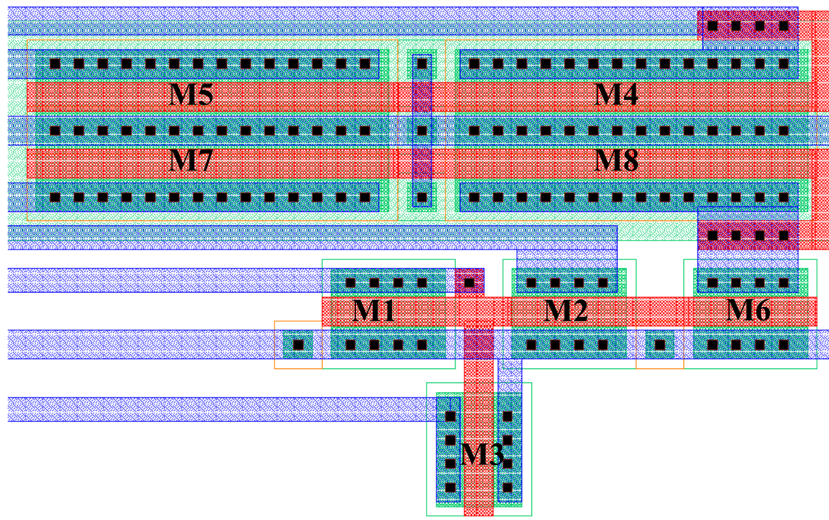


Figure 1: Transistors used to measure the effects of oxide encroachment, process variation, and the differences in transconductanceand channel length modulation between nFETs and pFETs.



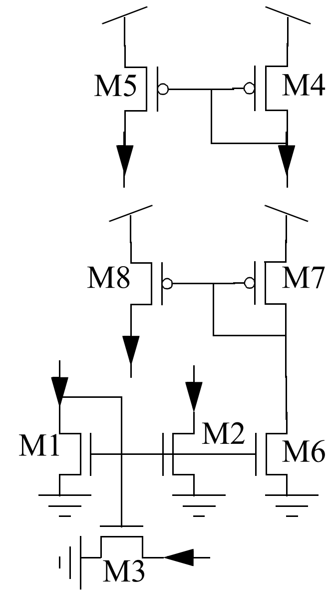


Figure 2: Circuits used to measure the effects of transistor mismatch on current mirrors. The block consists of four different current mirror circuits (M1-M2, M1-M3, M4-M5, and M1-M6-M7-M8).

Second, the students are asked to examine the layout of the *basic current mirror mismatch block*, shown in Figure 2, draw the corresponding circuits (also shown in Figure 2), and rank the four current mirror circuits (A:M1-M2, B:M1-M3, C:M4-M5, and D:M1-M6-M7-M8) in the order of increasing mismatch between the input and output current.

Third, the students are asked to examine the layout for the *scaled current mirror block*, shown in Figure 3, draw the corresponding circuits (also shown in Figure 3), and predict which layout technique, (I) or (II), will produce an output closer to the expected value.

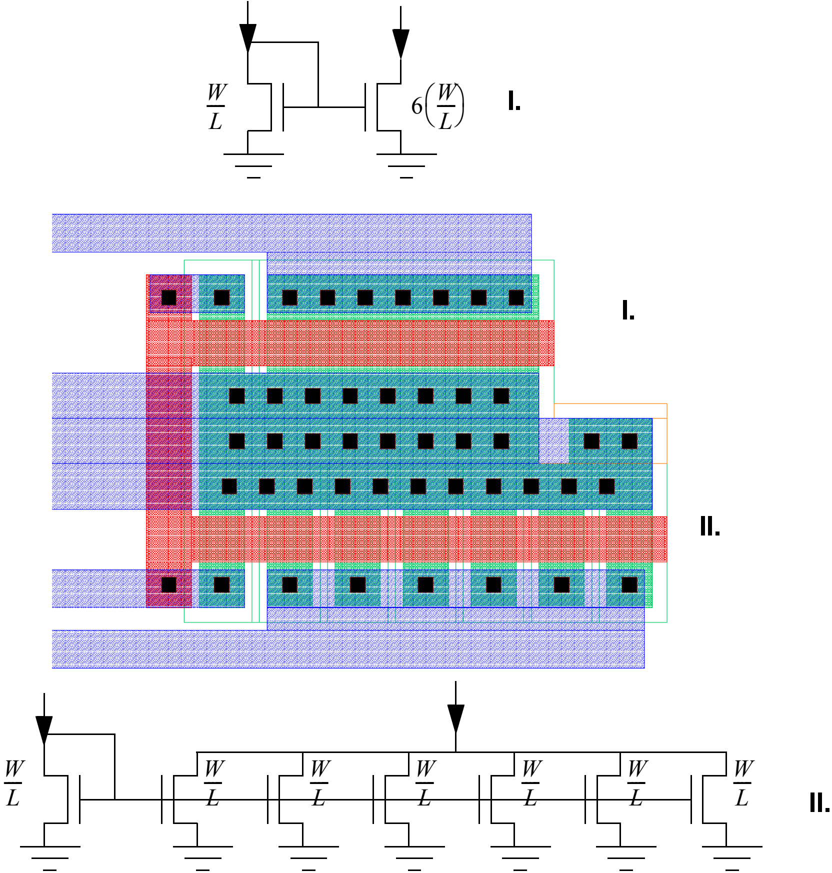


Figure 3: Circuits used to demonstrate different methods of scaling the output current of a current mirror.

Finally, the students are asked to examine the layout for the *current mirror array block*, shown in Figure 4, and rank which layout technique (I, II, or III) will produce the least amount of deviation among the outputs.

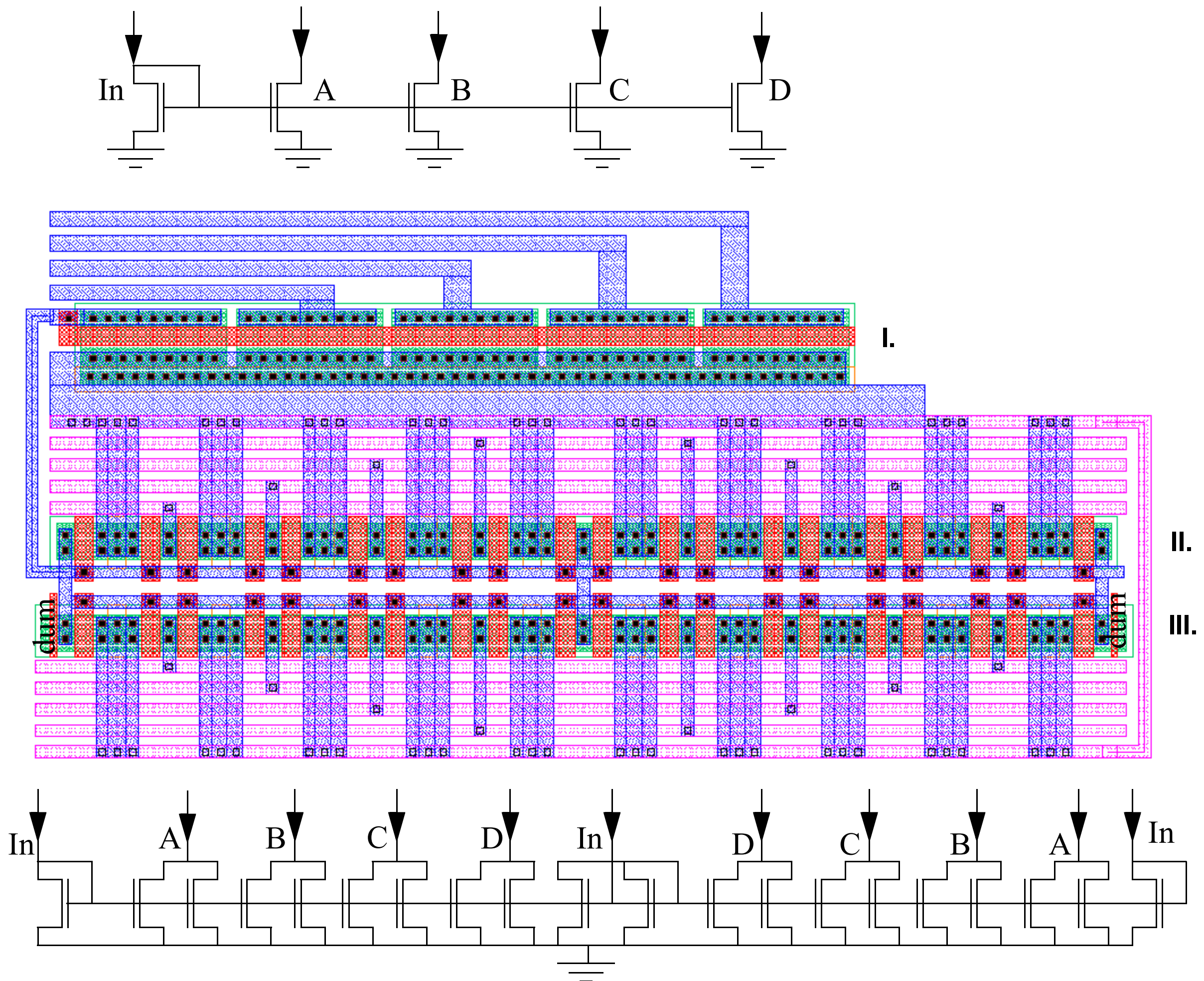


Figure 4: Three different methods of laying out a current mirror array. The first method, shown as circuit I, produces 4 copies of the input current. The second method, circuit II, arranges the 4 output stages in a common centroid configuration. The third method, circuit III, uses a common centroid layout with dummy lines on the ends.

Hardware Lab

There are four parts to the hardware lab, which involve the students testing each of the four circuit blocks. The first experiment, which uses the *transistor mismatch block* shown in Figure 1, tests the output current of the individual FETs with the gate voltage and the output voltage (V_{DS}) tied to $V_{DD}/2$=2.5V. If all process parameters were identical, the output currents of all FETs should be identical. However, because the transconductance of the nFETs is greater than the transconductance of the pFETs ($K_N > K_P$) the nFET currents are greater than the pFET currents. In addition, due to oxide encroachment, the output current for the nFET with W/L=27/18 is greater than the

output current for the nFET with W/L=3/2 ($I_{N27/18} > I_{N3/2}$), and similarly, the output current for the pFET with W/L=27/18 is greater than the output current for the pFET with W/L=3/2 ($I_{P27/18} > I_{P3/2}$). The output currents are compared between the transistor sets on each side of the chip, where small differences in output current are exhibited among identical transistors due to variation in oxide thickness and doping. Next, the students repeat their measurements when the output voltage is raised to 3V. This experiment allows the students to measure the channel length modulation for each FET and compare the resulting λ values. It also reinforces the difference between output voltage, which is relative to ground, and source-drain voltage, which is relative to the source voltage, since the output current increases for the nFETs and decreases for the pFETs. The channel length modulation is worse for pFETs than nFETs, as expected, however our experiments also demonstrated an increase in channel length modulation with W/L (i.e. $\lambda_{N27/18} > \lambda_{N3/2}$), which was unexpected. We are still seeking explanations for this unexpected result.

The next experiment, which uses the *basic current mirror mismatch block*, examines the mismatch among the four basic current mirror pairs shown in Figure 2. The input voltage and the output voltage for each current mirror are set to $V_{DD}/2$=2.5V to eliminate the effects of channel length modulation. The input current and the output current are measured and the percent error is calculated for each mirror circuit. The input current is independently measured for each pair so that the students may obtain a precise calculation of the error. The students then compare the mismatch among the different circuits and compare the experimental results to their prelab predictions. The results obtained by our experiments are shown in Figure 5.

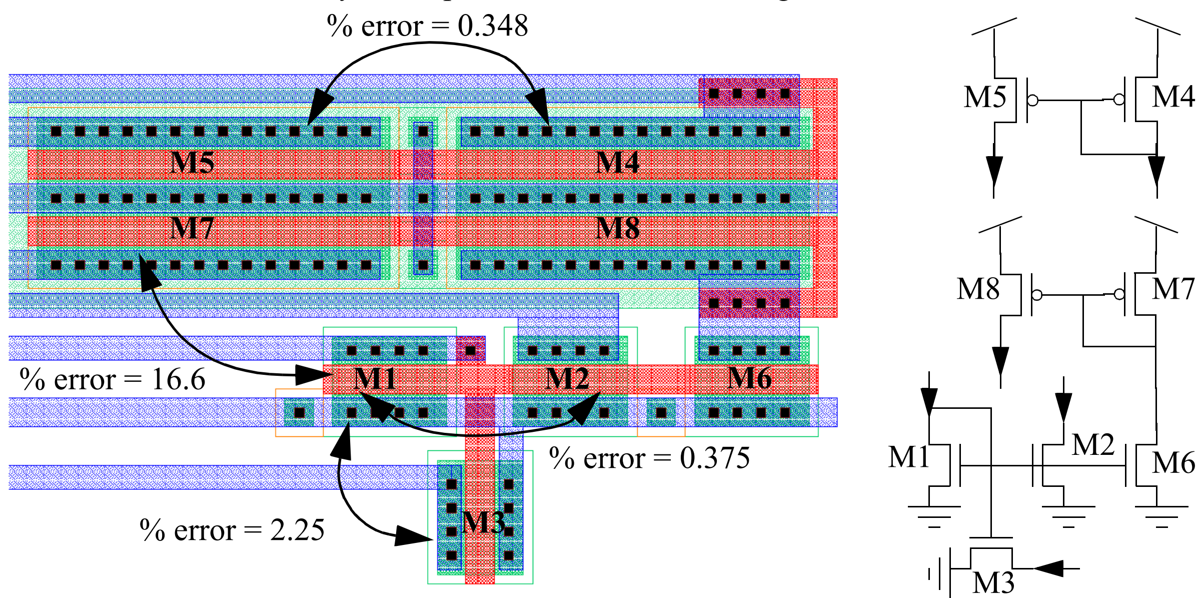


Figure 5: Percent error for each current mirror circuit. Merely changing the orientation of the output FET increases the error by almost 10%.

Another experiment that may be performed on this block that was not included in the lab due to time constraints helps the students understand the nature of the floating node between M6 and M7. The students may decrease the gate voltage of M4 and the output voltage of M5, keeping

these two voltages equal, until the pFET current mirror pair produces the same current as the nFET current mirror pair. This voltage should equal the voltage of the floating node between M6 and M7. The students may then decrease the output voltage of M8 to the same value, effectively eliminating the effects of channel length modulation between M7 and M8. The matching should improve.

The third experiment, which uses the s*caled current mirror block* shown in Figure 3, tests the effects of scaling the input current by scaling the W/L ratio of the output FET (circuit I.) versus scaling the input current by using multiple copies of the input FET (circuit II). The input voltage and the output voltage are set to $V_{DD}/2=2.5V$ to eliminate channel length modulation and input and output currents are measured for each circuit. The input current is independently measured for each pair so that the students may obtain a precise calculation of the error. The ideal output current is calculated as 6 times the input current and the resulting percent error is calculated. Our experiments measured a 65% error in circuit (I). and a 6.7% error in circuit (II).

The final experiment, which uses the *current mirror array block* shown in Figure 4, tests the three methods of laying out a current mirror array. The input and output voltages are set to $V_{DD}/2=2.5V$ to eliminate channel length modulation and the input current and each of the four output currents are measured for each circuit. The worst case percent error and standard deviation for each circuit are calculated by the students. Our experiments demonstrated the following mean and standard deviations for each of the circuits. In addition, some chips will provide an excellent example of

	mean	std dev
circuit I	975µA	5.69µA
circuit II	774µA	1.01µA
circuit III	762µA	2.16µA

process variation. The output currents for circuit (I) will increase or decrease monotonically, showing a linear process variation.