

Summary and Expected Results for the Mirrors Hardware Lab

Summary of the Chips

Our analog and mixed-signal VLSI course uses two hardware labs. The mirrors lab demonstrates the effects of mismatch and oxide encroachment on transistors and current mirrors. The students experiment with individual transistors and three different sets of mirror circuits to obtain a hands-on experience with some of the limitations of integrated circuit processing. The chip has been fabricated using the AMI 0.6 μm process and are contained in the area of a Tiny Chip (1500 μm X1500 μm).

Individual MOS Transistor Mismatch: The first set of experiments deals with two sets of identical transistors that are placed on opposite sides of the chip (set A and B as shown in Figure 1) that may be used to investigate the effects of process variation on the output current. The gates of all nFETs and pFETs in each set are tied together. Individual transistor output currents may be measured with a current meter. Each set contains two nFETs and two pFETs that have the same W/L ratio, but different values of W and L [i.e. $W/L_2 = (9W_1)/(9L_1)$]. Theory indicates that the output current should be the same if V_{DS} is the same, given that the gates are tied together. However, this theory does not prove to be true due to oxide encroachment. Each set also contains nFETs and pFETs with the same W/L ratios so that the effects of electron versus hole mobility and differences in channel length modulation may be observed.

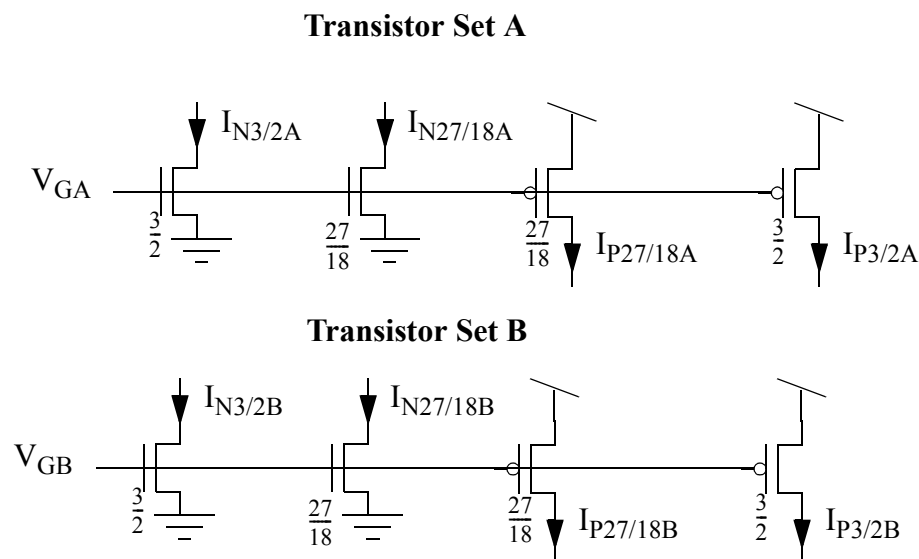


Figure 1: Two sets of identical transistors (set A and set B) placed on opposite sides of the chip used to investigate the effects of transistor mismatch.

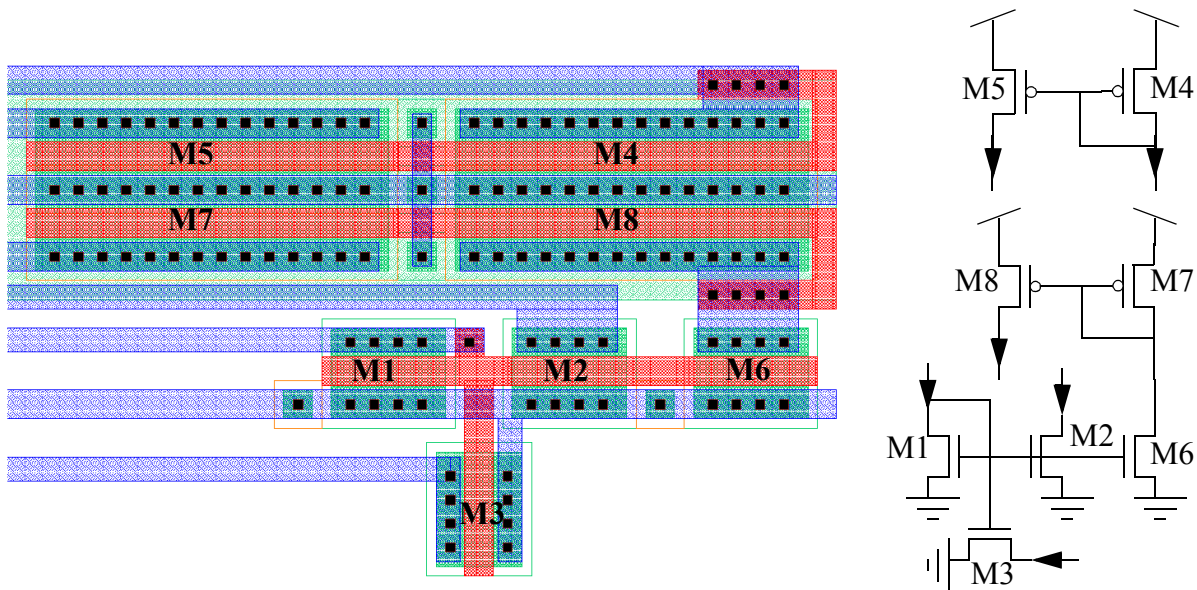


Figure 2: Circuits used to measure the effects of transistor mismatch on current mirrors. Four different experiments are performed using this circuit.

Basic Current Mirror Mismatch Circuits: These circuits allow the students to experiment with the mismatch in current mirrors. M1 and M2, as shown in both the layout and schematic in Figure 2, make up a standard nFET current mirror. The students can compare the input and output current and measure the best current matching that they can obtain on the AMI 0.6 μ m process. M1 and M3 also make up a standard nFET current mirror pair with the output transistor in a different orientation than the input transistor. Experimenting with this circuit allows the students to observe the effects of doping angle on transistor matching. M4 and M5 make up a pFET current mirror pair. The matching among nFET current mirror pairs can be compared to the matching among pFET current mirror pairs. M1, M6, M7, and M8 translate the current in a sink to a sourced current. This circuit allows the students to observe mismatch accumulation.

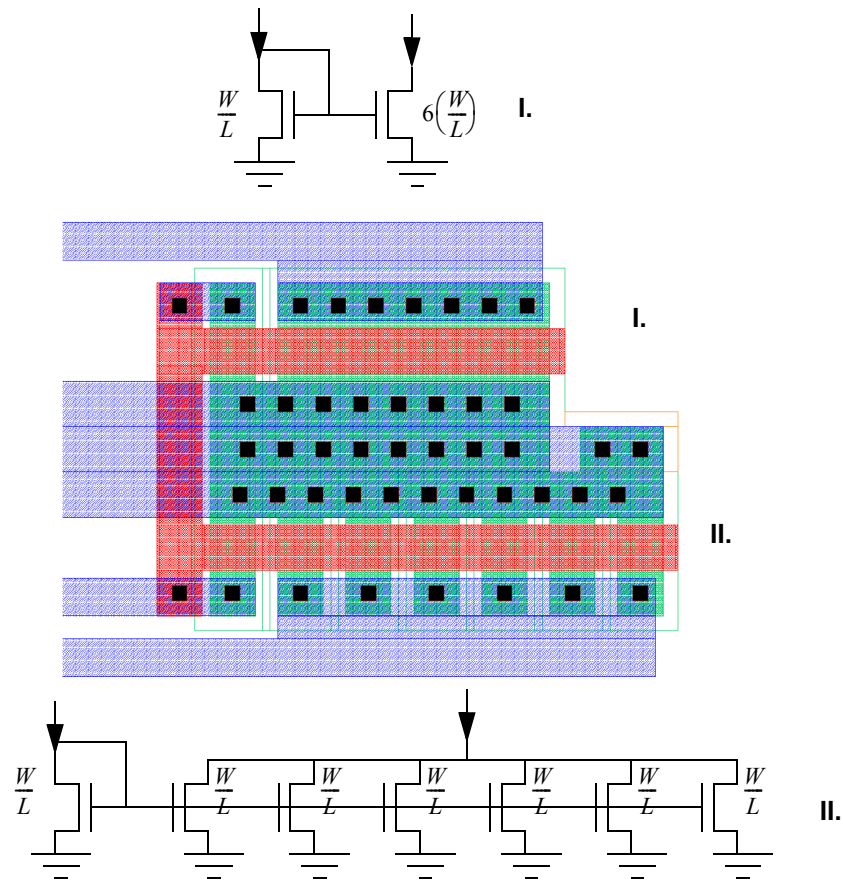


Figure 3: Circuits used to demonstrate different methods of scaling the output current of a current mirror.

Scaled Current Mirror Circuits: These circuits demonstrate the effects of two layout methods of scaling the output current of a current mirror. The first method, shown as circuit (I) in schematic and layout form in Figure 3, scales the output current by scaling the (W/L) ratio of the output transistor. The second method, shown as circuit (II), scales the current by using 6 transistors that are the same size as the input transistor connected in parallel. By experimenting with these two circuits, the students observe the effects of oxide encroachment on scaled FETs.

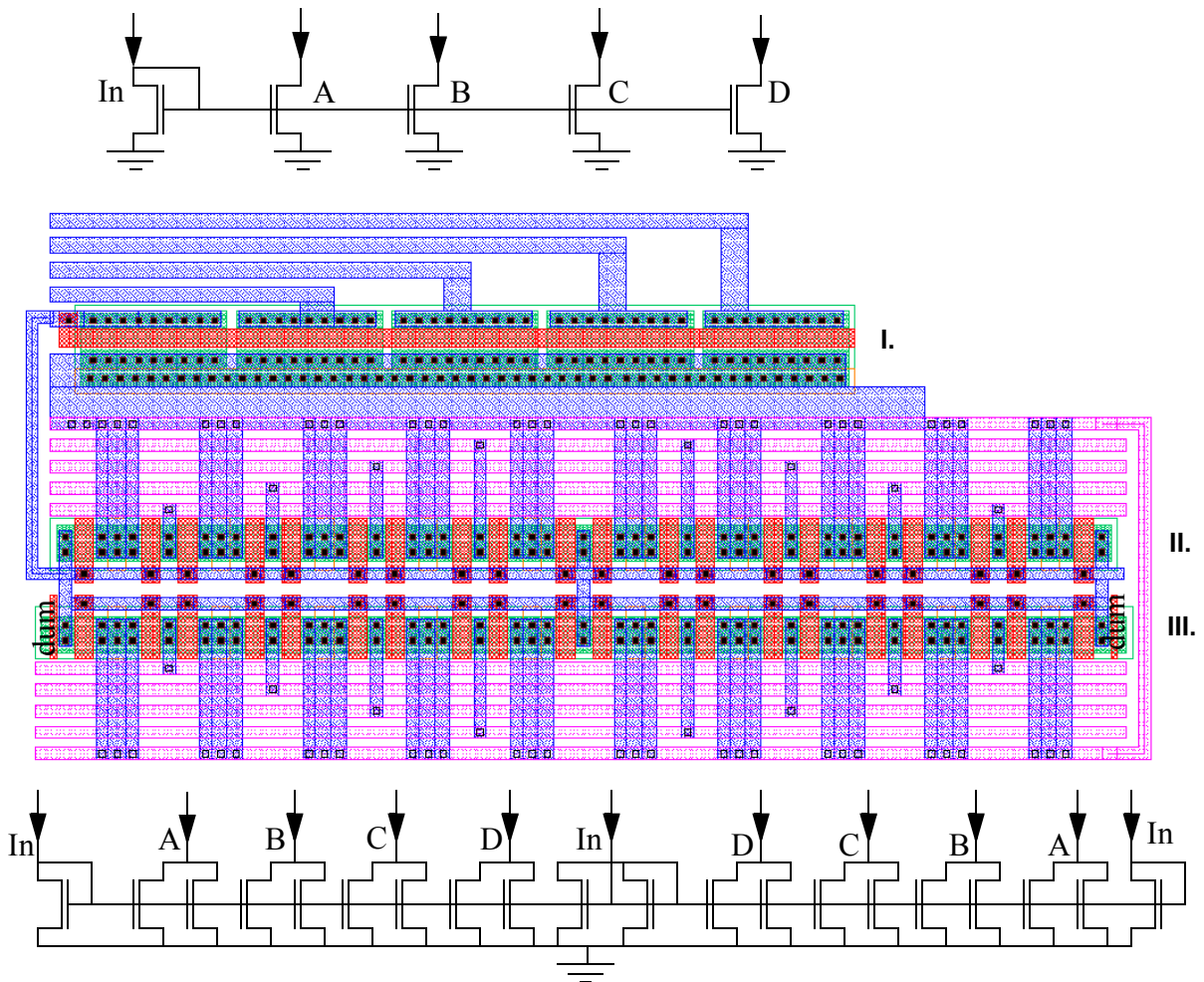


Figure 4: Three different methods of laying out a current mirror array. The first method, shown as circuit I, produces 4 copies of the input current. The second method, circuit II, arranges the 4 output stages in a common centroid configuration. The third method, circuit III, uses a common centroid layout with dummy lines on the ends.

Current Mirror Array Circuits: These circuits are used to demonstrate the effectiveness of different layout techniques used to minimize the effects of process variation on an array of current mirrors. Circuit (I), shown in Figure 4, is a standard nFET current mirror array that produces four copies of the input current. Circuit (II) is the identical circuit layed out in a common centroid configuration. The transistors in circuit (I) are replaced by 4 parallel transistors with widths that are 1/4 of the size of the transistors in circuit (I). These 4 parallel transistors are arranged in a common centroid configuration (AA BB CC DD DD CC BB AA), which should distribute the process variation of parameters more evenly among the different output stages. Circuit (III) uses the same common centroid layout as circuit (II) and adds dummy gates (labeled *dum* in Figure 4) to the outside edges of the array to minimize the overetching that often occurs to gates on the outside of an array.