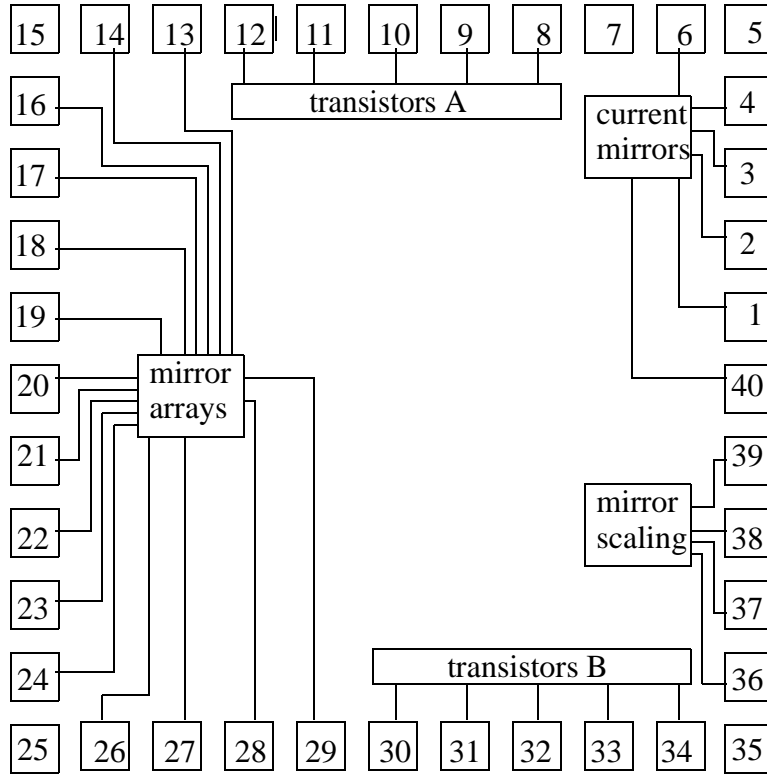


## PinOut



## Pin List

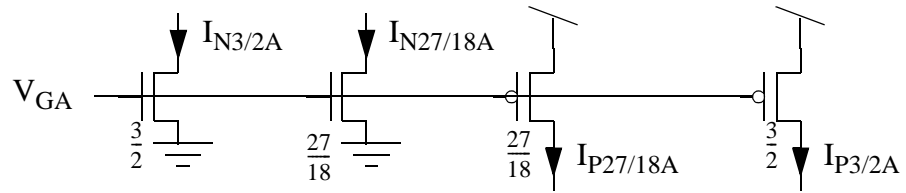
1: NmirIn	11: $I_{N27/18A}$	21: outBcc	31: $I_{N27/18B}$
2: NmirOut	12: $I_{N3/2A}$	22: outAcc	32: $V_{GB}$
3: NmirPout	13: outDmir	23: InCC	33: $I_{P27/18B}$
4: PmirOut	14: outCmir	24: InCCd	34: $I_{P3/2B}$
5: bias	15: gnd	25: Vdd	35: padVdd
6: PmirIn	16: outBmir	26: outAccd	36: InScaleM=6
7: X	17: outAmir	27: outBccd	37: InScale
8: $I_{P3/2A}$	18: InMir	28: outCccd	38: OutScale
9: $I_{P27/18A}$	19: outDcc	29: outDccd	39: OutScaleM=6
10: $V_{GA}$	20: outCcc	30: $I_{N3/2B}$	40: NmirSW

### Notes:

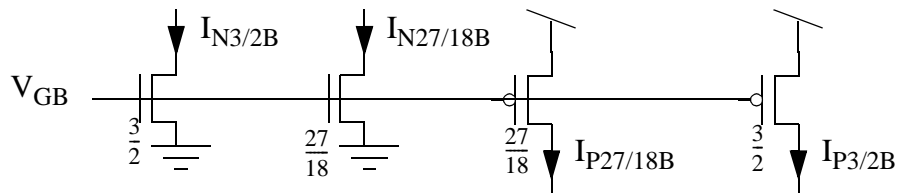
- *padVdd* and *Vdd* may be connected together.
- *bias* is not used in this circuit.

# Schematics

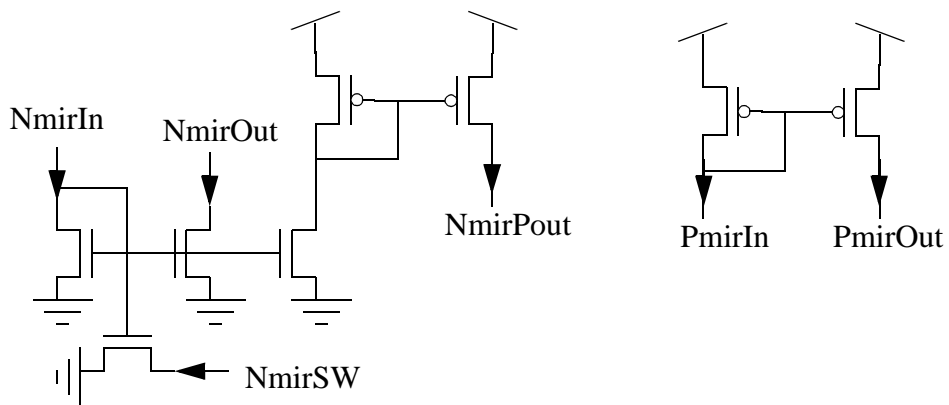
## Transistors A Schematic



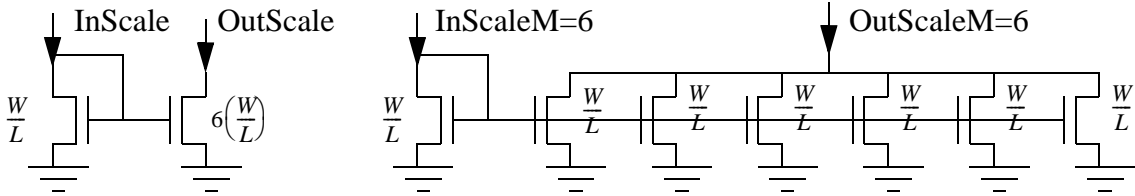
## Transistors B Schematic



## Current Mirrors Schematics



### Mirror Scaling Schematics



### Mirror Arrays Schematics

