

Summary and Expected Results for the Digital Hardware Lab

Summary of the Chips

The hardware lab for our digital VLSI course uses two integrated circuits, one demonstrating clock skew and the other demonstrating power-ground bounce. Both chips contain a large array of D flip-flops driven by a single, common input. Each flip-flop contains an inverter inside the flip-flop cell to produce the inverse of the clock signal. Both chips have been fabricated using the AMI 0.6 μ m process and are contained in the area of a Tiny Chip (1500 μ m X1500 μ m). Both fabricated chips are used with a single board and tested by the students to give them a hands-on experience with clock skew and power/ground bounce.

Clock Skew Chip: The clock skew chip uses an interdigitated layout for the power and ground rails of the flip-flop array and a serpentine layout for the clock, as shown in Figure 1. The interdigitated layout of the power and ground rails minimizes the power and ground bounce on this chip and provides an example of the proper method of laying out power and ground lines. The serpentine layout of the clock induces a large degree of clock skew along the array of flip-flops and provides an example of the improper method of layout out a clock line. The outputs of flip-flops connected along the length of the serpentine clock signal are taken off-chip to be observed by the students.

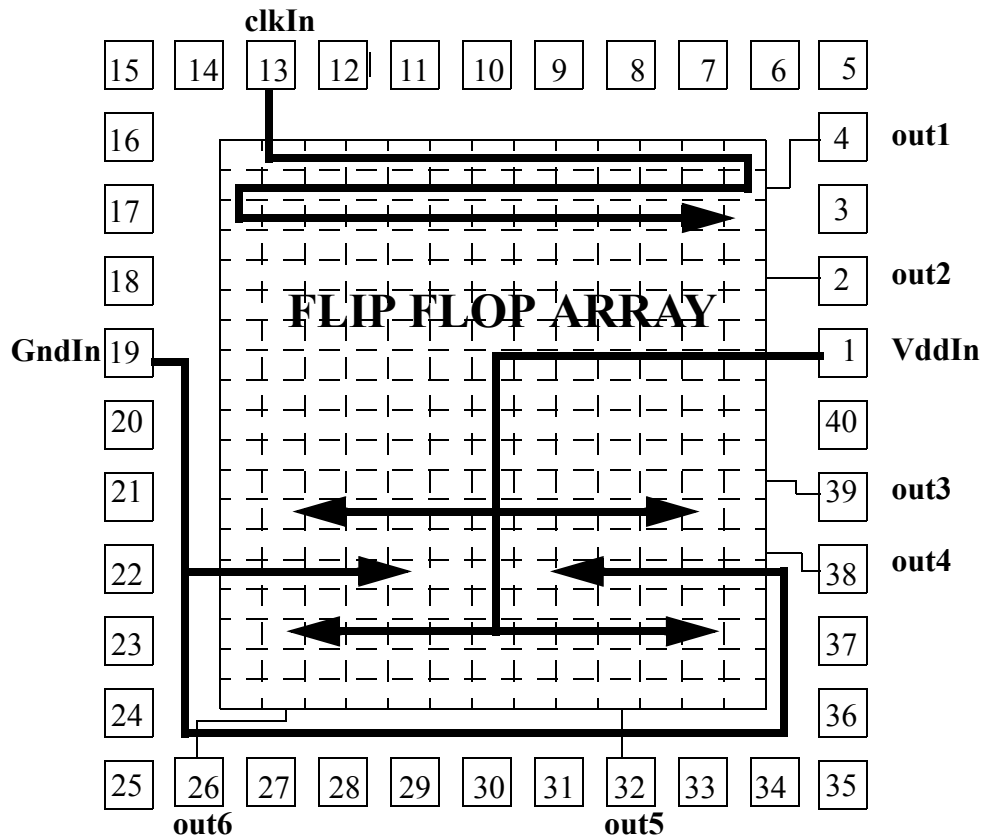


Figure 1: Clock skew chip. Array of flip-flops with clock layed out in a serpentine configuration and power and ground rails layed out in a interdigitatæd fashion.

Rail Bounce Chip: The power-ground bounce chip contains an H-tree distribution for the clock and a serpentine distribution for the rails, as shown in Figure 2. The H-tree distribution for the clock minimizes clock skew across the chip and ensures that all of the flip-flops are clocked at approximately the same time. The layout also provides an example of a proper method for laying out a clock line. The serpentine layout of the power and ground rails causes a large IR drop across the rail wires which induces power and ground bounce. This layout also provides an example of improper rail layout. This chip connects the outputs of several flip-flops along the length of the serpentine power signals to output pins so they may be observed by the students.

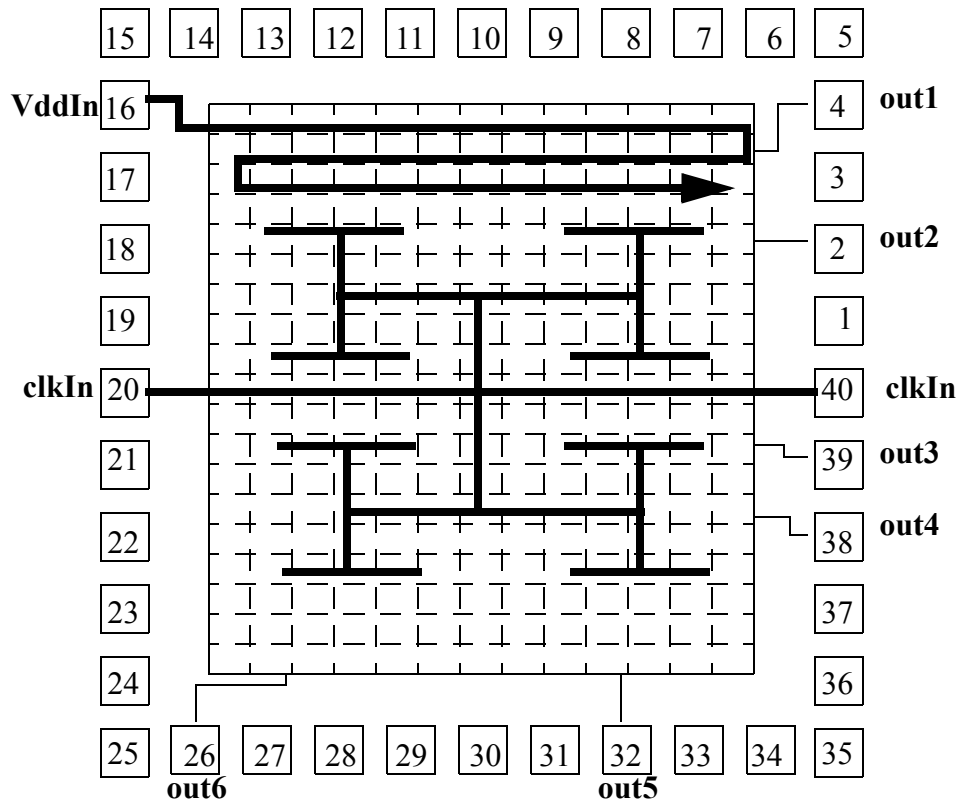


Figure 2: Rail bounce chip. Array of flip-flops with power and ground rails layed out in a serpentine configuration and clock line layed out in an H-tree distribution.