ECE Department
ECE250 – Electronic Device Modeling
Fall 2009

Instructor Information

Instructor: Marc E. Herniter
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CATALOG DESCRIPTION: *Modeling, analysis, and simulation of electronic circuits that contain two-terminal and three-terminal semiconductor devices. Large-signal, biasing, and small-signal analysis models. Introduction to wave shaping circuits, switch circuits, and amplifiers. Integral Laboratory.*

COURSE OBJECTIVES:
After successfully completing this course the student should be able to:

- Characterize 2 and 3 terminal devices by means of I-V plots.
- Derive a linearized small-signal model given the large signal characteristics.
- Describe a circuit and analyze its operation in terms of the bias and midband small-signal model, or its large-signal switching model.
- Use simulation tools to model a circuit and discuss the difference between the DC, time-domain, and frequency-domain analyses.
- Measure the DC characteristics of a 2 or 3 terminal device in the laboratory.
- Construct and test small rectifier and transistor circuits in the laboratory.
- Use elementary troubleshooting techniques and critical error analysis in the laboratory.
- Use standard written and oral formats to report laboratory/computation results.
- Demonstrate the similarity of operation between all 3 terminal devices that can be used as amplifiers or switches
- Show how three terminal devices can be used as switches or amplifiers.
- Emphasize single-stage amplifiers using topologies found in integrated circuits.
- Understand the impact of thermal and optical effects on semiconductor devices.
- Introduce the properties of semiconductor materials such as doping, carrier concentrations, conductivity, drift and diffusion current, and introduce a qualitative understanding of the device construction and operation.

PREREQUISITE: ECE200

PREREQUISITE SKILLS

1) KVL, KCL.
2) Circuit elements R, L, and C.
3) Thevenin and Norton Equivalents.
4) Independent and dependent voltage and current sources.
5) Ideal OP-AMP circuit analysis.

REQUIRED MATERIALS:

TEXTBOOK: *Schematic Capture With Cadence PSpice,2nd Edition*, M.E. Herniter, Prentice Hall, 2003. ISBN: 0-13-048400-8. (The first edition is O.K. if you already have it.)

TEXTBOOK: *Microelectronic Circuits*, Sedra and Smith, Oxford, 2004, 5th Ed., ISBN: 0-19-514251-9.

NOTEBOOK: National Brand Computation Notebook Number 43-648. Or any notebook with non-removable pages and page numbers is required.

REQUIRED SOFTWARE:

PSpice: OrCAD PSpice and Capture version 15.7. Instructions for installing the software are available on my website at http://www.rose-hulman.edu/~herniter/Rose_Classes/ECE351/351_index.htm.

EVALUATION METHOD:

Homework	.....	10%
Lab	.....	15%
Pre-Lab	.....	5%
Lab Practical Exam	.....	5%
Exams (3 at 20% each)	.....	60/3%

- Three exams will be given during the quarter. The third exam will be held during the time scheduled for the final.
- The final has the same weight as the two other exams. **The final exam will last three hours only.**
- A grade of incomplete will only be given for circumstances beyond a student's control. Class load, extra curricular activities, and jobs are all circumstances that are under the control of a student and will not justify a grade of incomplete.
- Your grade will be based on the following schedule
    - A : Total Average ≥ 92
    - B+: 92 > Final Average ≥ 87
    - B : 87 > Final Average ≥ 82
    - C+: 82 > Final Average ≥ 77
    - C : 77 > Final Average ≥ 72
    - D+: 72 > Final Average ≥ 67
    - D : 67 > Final Average ≥ 62
    - F : 62 > Final Average

EXAM SCHEDULE:

- Exam 1 – September 29, 2009 (Tuesday – Week 4)
- Exam 2 – October 29, 2009 (Thursday – Week 8)

COURSE POLICIES:

HOMEWORK: There will be 10 homework assignments (order of magnitude estimate). These assignments should be done independently. Homework is due at the beginning of class on the due date. Late homework will not be accepted. Solutions are available on my web site. The files are downloadable and can be viewed with the Adobe Acrobat Reader. **You are required to use the standard RHIT format for homework.**

ATTENDANCE: Attendance is required.

LATE HOMEWORK: Homework is due at the beginning of class on the specified due date. Late homework will not be accepted.

IN CLASS EXAMS: These exams are open book, open notes, and open brain (your brain only). Expect a difficult exam with an average near 50%. Personal computers may only be used during exams to view the class notes. You may not use Maple or PSpice during the exam.

HONOR CODE: The honor code will be enforced in this class.

MAKEUP EXAMS: Makeup exams will not be given.

LABORATORY: Lab grading will be discussed in the lab. You must bring the following items to the lab (starting the second lab period of the quarter):

- Nickels, dimes, and quarters to purchase parts.
- A breadboard. This can be purchased in the lab.
- A pre-cut prototyping wire kit.
- Hemostats.
- Your lab notebook.
- Glue. The preferred type is Elemer's Blue School Gel.
- Scissors.
- A Pen. Pencils are not allowed.

INSTRUCTIONAL PHILOSOPHY: Topics will be covered in three levels: Theoretical analysis, simulation, and laboratory verification. The following synthesis procedure is used to gain an understanding of circuits covered in the class: The theoretical analysis of the circuit is covered to understand the operation of the circuit or to design a circuit. Circuit simulation using industry standard analysis tools to verify the theoretical analysis or circuit design. If the simulations agree with theoretical analysis, the circuit is constructed in the lab. **Measurements of the circuit performance are made and compared to the theoretical calculations and simulation results.**

INSTRUCTIONAL OBJECTIVES

1. Semiconductor Physics (Ch. 1 of Neamen)
    - Insulators, conductors, and semiconductors.
    - Intrinsic and extrinsic semiconductors.
    - Carrier concentration, conductivity, drift and diffusion current.
2. Diodes
    - I-V characteristic
    - Temperature Effects
    - Iterative solution of simple series circuit
    - Solution of simple series circuit using an equation solver
    - PSpice solution of simple series circuit
    - PSpice I-V Characteristic
    - PSpice I-V Characteristic with temperature dependence
    - Load Line solution

- Thevenin solution

3. Diode Models (Covered with item 4.)
    - Ideal
    - Ideal with voltage drop
    - Ideal with voltage drop and series resistance
4. Diode Circuits
    - Rectifier
    - Clipping
    - PSpice simulation
5. Zener Circuits
    - Clipping
    - PSpice simulation
6. Bipolar Junction Transistors
    - PSpice AC, DC, transient, and bias point simulations
    - BJT as a switch
        - Drive an LED
        - Drive a relay
    - Biasing with Current Sources
    - BJT Small-Signal Analysis
        - Hybrid-pi model.
        - Common-emitter amplifier.
        - Emitter-follower.
        - Input and output impedance.
7. MOSFETS
    - PSpice AC, DC, transient, and bias point simulations
    - MOSFET as a switch
        - Resistive pull-up.
        - Active pull-up.
        - Drive an LED.
        - Basic NMOS gate.
        - Ohmic and SAT regions
    - Bias with Current Source
    - MOSFET Small-Signal Analysis
        - Small-signal model.
        - Common-source amplifier.
        - Source-follower.
        - Input and output impedance.
8. jFETs (Optional)
    - PSpice AC, DC, transient, and bias point simulations
    - Bias with Current Source
    - Ohmic and SAT regions
    - jFET Small-Signal Analysis
        - Small-signal model.
        - Common-source amplifier.
        - Source-follower.
        - Input and output impedance.