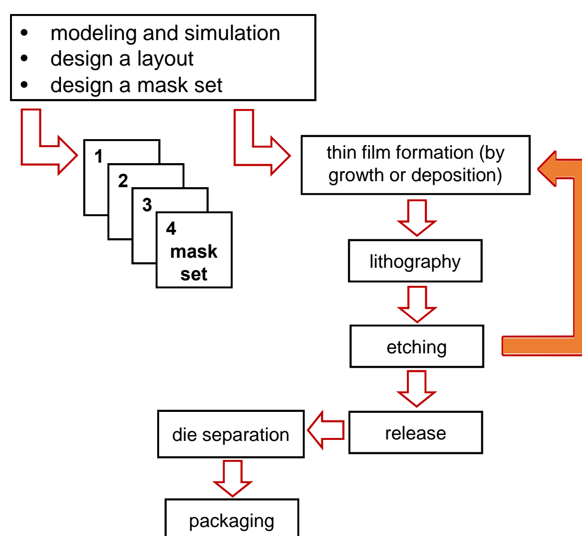
Process flow part 2

- ❑ Develop a basic-level process flow for creating a simple MEMS device
- ❑ State and explain the principles involved in attaining good mask alignment
- ❑ Identify and explain the various issues involved with designing good process flows

Typical process steps for surface micromachining



Mask design and layout

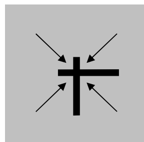
Mask layout

- The complete design with all mask layers combined is called the ______ of the device.
- Typically use software specifically designed for masks
- Program allows you to place mask layers on top of each other to ensure good alignment
- Each mask layer shown in a ___________________________________
- The software will separate the layers into the individual masks for fabrication.
- The software also keeps track of whether masks should be ________ or _________ depending on whether the process is typically __________ or _____________

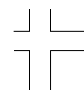
Mask design and layout

Mask alignment

Every mask *must* have alignment marks that will align the mask to the features on the wafer.



alignment feature on wafer



alignment feature on mask

mask aligned with wafer

Mask design and layout

Mask alignment

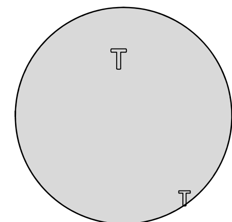
Issues to think about when designing the shape and the placement of the alignment mark:

- Does the alignment mark shape give ________________________ as well as alignment?
  - ______________ is good → a _________ is better than a "plus"
  - A ______ mask opening will produce a _____ etch in Si showing crystal directions. Align next masks to the *square*
- Make sure your mask does not obscure your alignment mark!
  -
  -
  -
  -

Mask design and layout

Mask alignment

- Use a variety of alignment marks
  - Use one large alignment mark one to get a sense of where you are on the wafer
  - Use smaller ones to fine tune the alignment
  - Use several marks ___________________. A small error in angle can _________ into a large error across the distance of the wafer



- Be sure your alignment mark is in a material you can see.
  -
  -
  -

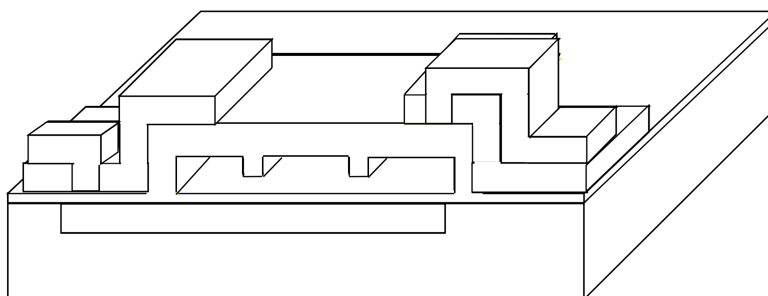
____________________ → first alignment mark

Mask design and layout

Mask alignment

- Know the process flow *of your alignment marks*
- Backside alignment

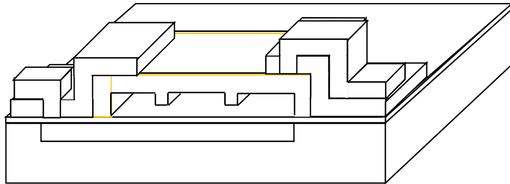
Surface μ-machined pressure sensor



- Silicon substrate
- Poly-Si diaphragm forms one plate of capacitor.
- n+ diffusion layer forms other "plate" of capacitor
- Aluminum wires send capacitive electrical signal off the chip.
- Oxide layer insulates aluminum wires from rest of chip
- Nitride insulates poly-Si diaphragm from n+ diffusion.
- Notches to prevent uncompensated stresses from breaking diaphragm during release

Process flow, pass 1

We can go through this example a little quicker.



What are the major steps to create the device?

1.

2.

3.

4.

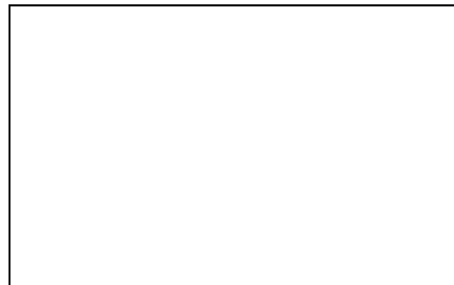
5.

6.

Detailed process flow

1. Diffusion of n+ dopant for bottom "plate" of capacitor
   a.
   b. Mask 2 – what does it look like? (Assume positive resist.)
   c. Breakdown of this step:

Mask 2



2. Deposit nitride

Detailed process flow

3. Deposit sacrificial oxide
   a. No mask is required since it covers the entire wafer
   b. Why cover the whole wafer? Why not pattern oxide to go just under the diaphragm and nowhere else?

4. Add poly-Si diaphragm
   a. How do we produce notches and pedestals? We will need two different etches.
   b. What will our etch stop method be?

   c. Breakdown of this step:

Mask 3

Mask 4

Mask 5

Detailed process flow

5. Sacrificial etch
   a. If using oxide for both sacrificial layer and insulation for the wires, need to do sacrificial etch ________ laying the oxide for the wires. Why?
   b. ________________ *requires* release to be done last. Why? How would we change our process flow if we have to do contact lithography?

6. Create wires
   a.

   b.

   c.

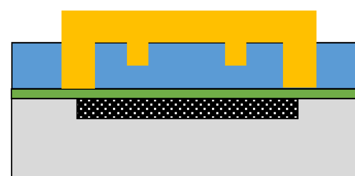
   d.

   e.

   f.

Mask 6

Mask 7



Final process flow

Final Process Flow for Surface Micromachined Pressure Sensor

Starting material: 100mm (100) p-type silicon, 1×10^{15} cm^{-3} boron with a 10 mm n-type epilayer, 5×10^{16} cm^{-3} phosphorus

1. **Clean:** Standard RCA cleans with HF dip
2. **Photolithography:** Mask 1 (alignment)
3. **Etch:** Etch alignment marks into Silicon.
4. **Strip**: Strip photoresist
5. **Photolithography:** Mask 2 (n^+ diffusion)
6. **Implant:** Ion implantation of phosphorous
7. **Strip:** Strip photoresist
8. **Clean:** RCA cleans, no HF dip
9. **Drive-in:** Drive in diffusion
10. **Clean:** RCA cleans, no HF dip
11. **Nitride:** Deposit insulating nitride layer
12. **Oxide:** Deposit sacrificial SiO_2
13. **Photolithography:** Mask 3 (notches)
14. **Etch:** Short etch to get notches
15. **Strip:** Strip photoresist
16. **Photolithography:** Mask 4 (pedestals)
17. **Etch:** Longer etch to get pedestals
18. **Strip:** Strip photoresist
19. **Clean:** RCA cleans, no HF dip
20. **Polysilicon:** Deposit polysilicon for diaphragm
21. **Photolithography:** Mask 5 (diaphragm)
22. **Etch:** Etch polysilicon
23. **Strip:** Strip photoresist
24. **Sacrificial etch:** Remove oxide leaving pedestal
25. **Clean:** RCA cleans, no HF dip
26. **Oxide:** Deposit SiO_2 for insulation
27. **Photolithography:** Mask 6 (vias)
28. **Etch:** Etch oxide to get vias
29. **Strip:** Strip photoresist
30. **Clean:** RCA cleans, no HF dip
31. **Metal:** Deposit aluminum for wires
32. **Photolithography:** Mask 7
33. **Etch:** Etch Aluminum
34. **Strip:** Strip photoresist
35. **Sinter:** Anneal contacts

Other issues in process flow

Other issues in designing good process flows

System partitioning:

-
-

Process partitioning:

-
-

Backside processing

-
-

Thermal constraints

-
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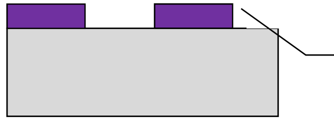
Other issues in process flow

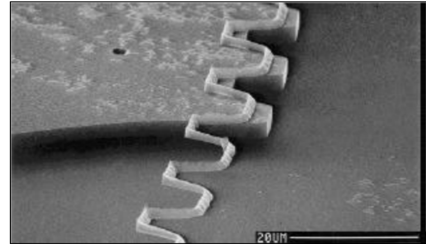
Other issues in designing good process flows

Device geometry

- Hard to visualize the 2-D and 3-D aspects of devices →
- Combination of conformal deposited layers with directional etching can result in ___________



- Can use _____________________ to avoid stringers, depth of focus problems, and other issues arising from large changes in topography



An example of a "floating stringer" (Courtesy of Sandia National Laboratory

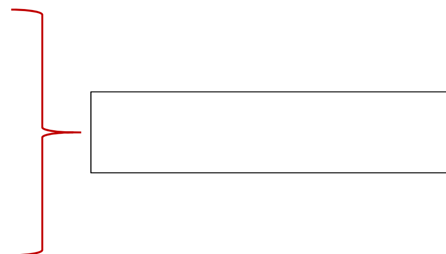
Other issues in process flow

Other issues in designing good process flows

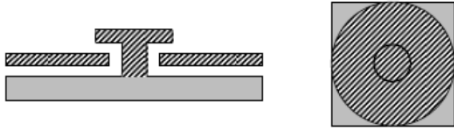
Mechanical stability:

Process accuracy:

-
-
-
-



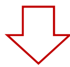
Other issues in process flow

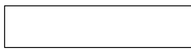


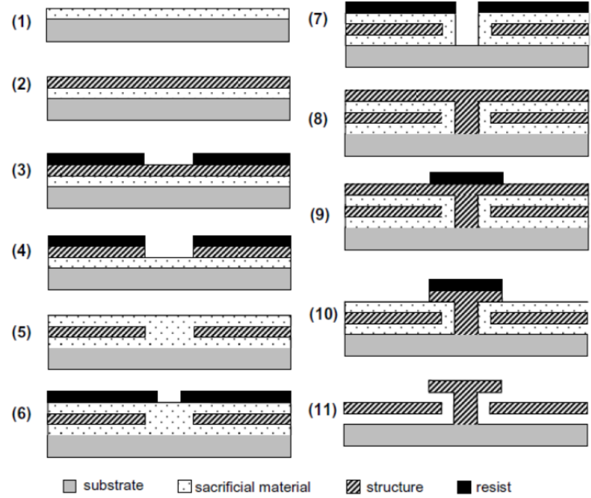
A MEMS wheel and hub

If using a ______ _________ in step 7

isotropic or anisotropic







A win-win process flow

The self-aligned gate transistor