Panel 1

Prior to class video lecture

Logic Gates

ME430 Mechatronics

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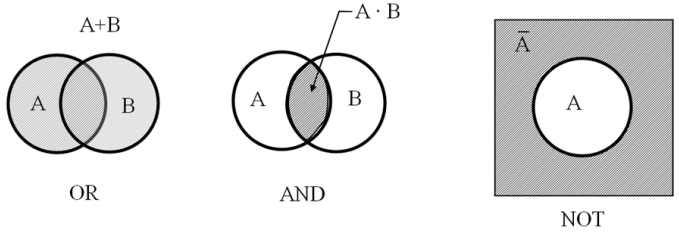
Panel 2

Table 1: Definitions for discrete Logic

True	False
Logic True = 1	Logic False = 0
In Circuits True is often = 5 volts	In Circuits False is = 0 volts
High	Low
On	Off

2

Panel 3



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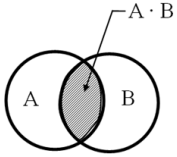
Panel 4

A	B	A · B
0	0	
0	1	
1	0	
1	1	

AND Gate:



AND

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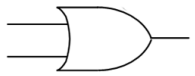
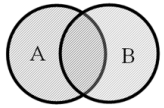
Panel 5

A	B	A+B
0	0	
0	1	
1	0	
1	1	

OR Gate:



A+B



OR

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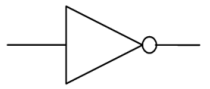
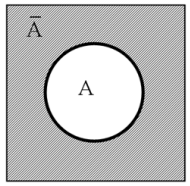
Panel 6

A	$\bar{A}$
0	
1	

Inverter (NOT gate):





NOT

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Panel 7

Most importance: NOT
AND
Least importance: OR

Example: Complete the truth table for the Logical Expression: $\overline{X+\bar{Y}\cdot Z}$

X	Y	Z	$\bar{Y}$	$\bar{Y}\cdot Z$	$X+(\bar{Y}\cdot Z)$	$\overline{X+\bar{Y}\cdot Z}$
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

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Panel 8

Most importance: NOT
AND
Least importance: OR

Example: Complete the truth table for the Logical Expression: $\overline{X+\bar{Y}\cdot Z}$

X	Y	Z	$\bar{Y}$	$\bar{Y}\cdot Z$	$X+(\bar{Y}\cdot Z)$	$\overline{X+\bar{Y}\cdot Z}$
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

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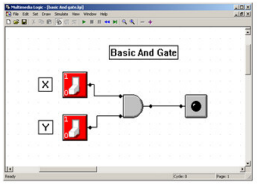
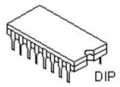
Panel 9

The two ways we'll play with Logic Gates:

1. Simulation - Using Multimedia Logic (MML)



2. Hardware - Using the 74_## Discrete Logic DIP Chips



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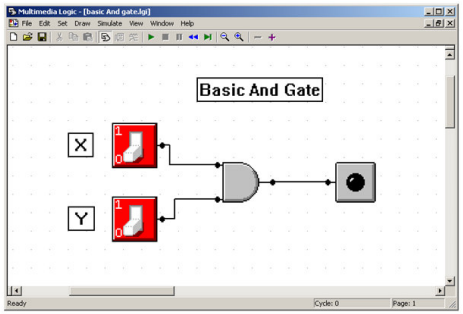
Panel 10

Let's go play with Multimedia Logic



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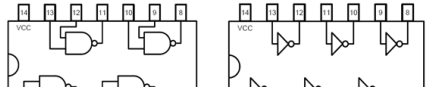
Panel 11

Digital IC chips:
Up until now, we've been talking about these logic gates as useful but vague mathematical or logical abstractions.

Some of the commonly available logic chips include:

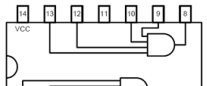
7400	Quad 2-Input NAND Gate
7402	Quad 2-Input NOR Gate
7404	Hex Inverter (NOT Gate)
7408	Quad 2-Input AND Gate
7410	Triple 3-Input NAND Gate
7411	Triple 3-Input AND Gate
7420	Dual 4-Input NAND Gate
7421	Dual 4-Input AND Gate
7427	Triple 3-Input NOR Gate
7430	8-Input NAND Gate
7432	Quad 2-Input OR Gate
7442	BCD to Decimal 4 to 10 Line Decoder
7446	BCD to 7 Segment Decoder/Driver
7454	4-wide AND-OR-Invert Gate
7473	Dual J-K Flip-Flops with Clear
7474	Dual D Flip-Flop with Clear and Preset
7486	Quad 2-Input XOR Gate
7489	64 bit Read/Write Memories
7490	Decade Counters
7491	8-bit Shift Registers
7493	4-bit Binary Counters
74138	3 to 8 Line Decoder/Multiplexer



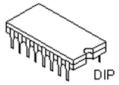
7400 Quad 2 Input NAND

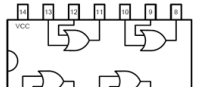
7404 Hex Inverter

7408 Quad 2 Input AND



7421 Dual 4 Input AND





7432 Quad 2 Input OR

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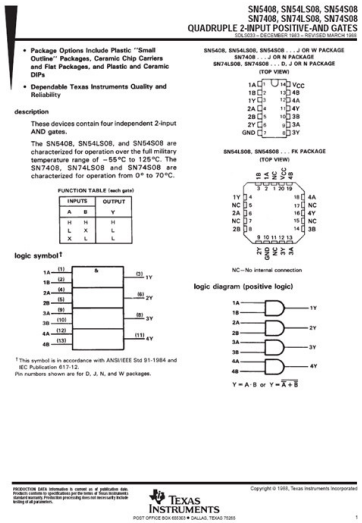
Panel 12

Go visit course website



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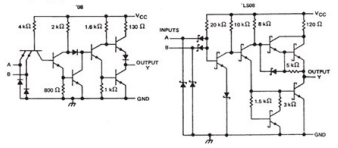
Panel 13

SN5408, SN54LS08, SN54S08
SN7408, SN74LS08, SN74S08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

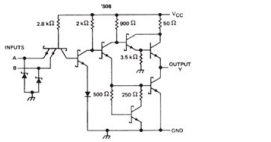
schematics (each gate)

'08



'LS08

'S08



Resistor values are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '08, 'S08 . . . . . 5.5 V
'LS08 . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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Panel 14

SN5408, SN54LS08, SN54S08
SN7408, SN74LS08, SN74S08
QUADRUPLE 2-INPUT POSITIVE-AND GATES

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.8			−0.8	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5408			SN7408			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −0.8 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 4.5 V		11	21		11	21	mA
I_{CCL}	V_{CC} = MAX, V_I = 0 V		20	33		20	33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		11.5	27	ns
t_{PHL}					12	19	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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