ECE 333: Digital Systems

Fall Quarter 2003

Instructor: J. Brandon Laflen

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Meeting Times: Class: M, T, Th 10:50-11:40 am
                       Lab: W 9:55 am - 12:35 pm

Required Text: Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design,* McGraw-Hill Companies, Inc., 2003.

Prerequisites: ECE130: Introduction to Logic Design
                       ECE200: Circuits and Systems
                       ECE250: Electronic Device Modeling

Lab Tools: Cadence Design Suite (available on sliderule, which can be connected to from the lab machines via X-Win32 v. 5.4)

                       Xilinx Foundation Series (available on the lab computers)

Office Hours: 7th and 8th hours, all week (or feel free to just drop in)

Course Description

This course is intended to provide you with the experience of building digital systems with time-to-market as a primary component. ECE130 provided you with the building blocks of digital systems. In today's industry, large systems are never implemented using discrete components. They are typically designed by one of two methods: either an integrated circuit is designed [subject of the VLSI course (ECE551)] or an existing integrated circuit that may be programmed is used [a programmable logic device (PLD)]. This course will focus on designing digital systems by programming PLDs using the hardware description language Verilog. Once you have a basic understanding of the Verilog hardware description language, we will then turn our focus to the analog nature of digital circuits. While ECE130 treated the output of all digital components as 1's and 0's, all clocks as perfect square waves, and all gates as having no delay, this course will address the fact that all digital gates are made out of analog transistors. The analog characteristics of the gates limit the maximum speed of the circuit, effect how many gates can be connected together, and cause noise to be induced from one circuit to another. It is in conquering these analog realities that state of the art, high-speed, low-noise designs are created. We will wrap up the quarter spending a little more time discussing other PLDs not covered in the lab.

In conjuction with the course material, we will have an accompanying lab where you will learn how to program two different kinds of PLDs to implement small digital systems. In addition, you will have an individual project where you will implement a significant digital system using a

field programmable array (FPGA) board that contains a PLD and additional hardware, such as seven-segment displays, I/O ports, etc.

Course Objectives

By the end of this course, I expect that you will be able to:

- Design the combinational and sequential logic for digital systems from a problem statement

- Write Verilog code describing combinational and sequential systems

- Write a testbench for a digital system using Verilog

- Successfully program GAL and FPGA chips

- Design basic CMOS logic structures using transistors

- Calculate the AC and DC charateristics of a logic gate

- Design a circuit that will control a given I/O port at a required speed

- Design circuits that minimize crosstalk, interference, and transmission line effects.

General Policies

Homework: Homework assignments will be assigned weekly. Late homework will not be accepted unless arrangements have been made prior to the deadline, with the possible exception of extenuating circumstances (at my discretion). If solutions have been posted, assignments will be returned ungraded. I must be able to follow your work easily; please write clearly and neatly. Your grade is not just a function of knowing the material, but also of being able to communicate it clearly. Sketches, schematics, and plots must be neat and labeled clearly.

Laboratory: The laboratory will be held in B200. Lab is a group effort, and therefore labs grades will be assigned to the entire group. Each partner must obtain a lab notebook. The lab notebook is to be a running record of your work in lab, including the assigned "prelab" activities. Do the prelab work in your lab notebook. Submit a **copy** of your prelab notebook pages at the beginning of the class period the day before lab. Rotate the duties for maintaining the lab notebook each lab period. Lab notebooks for a given lab will be collected at the beginning of the following lab period. Missed lab work MUST be made up regardless of the reason the lab was missed. A late penalty of 10% grade reduction per day will apply unless previous arrangement for absence have been made. The instructor has the option to reorganize the lab groups.

The lab notebook is meant to contain more than your final design. Many designs go through iterations. Please keep all iterations of a design in your lab notebook. Sometimes, when you get to lab, you find that a previous iteration may have been a better solution, and you wish you had that design with you. If you write everything in your lab notebook, you will have everything that you need. The lab notebook is also meant to be a detailed account of your testing. Be sure to write down ALL pertinent information in your testing proceedure so that another student could reproduce the experiment by merely reading your lab notebook. Make sure that all schematics, diagrams, and graphs are clearly labeled. Both axes should be labeled, and if you have multiple waveforms on a single graph, you should clearly indicate what each output is so that it is consistent with your schematic. The lab reports are meant to make you think about the material

that you have been learning. I want you to report not just what you observed, but explain why you think the observations occured. Thought process is more important than a single "right" answer.

In-class Quizzes and Participation: Because of the design nature of this course, I will facilitate group work whenever possible. By working and learning together in groups, we will simulate a design atmosphere more consistent with industry. From time to time I will expect each student to participate in class by solving problems at the board, contributing within a group, or demonstrating a particular concept through an in-class quiz. Please come to class prepared! If you keep up with the course-assigned reading and weekly homework and laboratory assignments you will be in an excellent position for class participation and for grasping more complex concepts.

Exams: There will be three quarter exams. The third quarter exam will be administered during the final exam period. However, this exam will not be cummulative and will count equally with the two exams given during the quarter. The exact dates for these exams are given on the course outline. You must talk with me BEFORE the exam if you have a conflict so that suitable arrangements can be made. Exams missed due to an unexcused absence cannot be made up.

Grading Policy:	Homework:	5%
	In-class:	5%
	Prelabs:	5%
	Lab notebooks:	10%
	Exams (3):	20% each
	Design Project:	15%

The cumulative exam score must be at a passing level (i.e. $>= 60\%$) in order to pass the course.

All lab work (prelabs, lab notebooks, and design project report) must be submitted in order to pass the course.