ECE333-01 Tentative Course Schedule - Winter 2003-2004

Week	Day	Date	Topic	Recommended Reading	Due-Dates
1	Mon	1-Dec	Course Overview	Chapt 1	
	Tue	2-Dec	Review Digital Logic: Combinational Circuits	2.1-2.8,4.1-4.5 & 5.3,6.1,6.2,6.5	Prelab 1
	Thur	4-Dec	Lab 1		
	Fri	5-Dec	Review Digital Logic: Sequential Circuits, finite state machines	7.1-7.6,7.8,7.9 & 8.1-8.3, 8.7	
2	Mon	8-Dec	Verilog HDL	2.1	HW1
	Tue	9-Dec	Combinational Circuits	*Gradual Intro to Verilog: Combinational,* & 6.6	Prelab 2
	Thur	11-Dec	Lab2		Lab 1
	Fri	12-Dec	Simulation Techniques for Combinational Circuits	class demo	
3	Mon	15-Dec	Sequential Circuits	*Gradual Intro to Verilog: Sequential* & 7.12-7.14	HW2
	Tue	16-Dec	Simulation Techniques for Sequential Circuits	class demo	Prelab 3
	Thur	18-Dec	Lab3		Lab 2
	Fri	19-Dec	**Exam 1**		
Winter Break			December 20 - January 4		
4	Mon	5-Jan	Handshaking Between FSMs and Asynchronous Inputs	10.3.3	HW3
	Tue	6-Jan	Data Path/Controller Partion	10.2	Prelab 4
	Thur	8-Jan	Lab4		Lab 3
	Fri	9-Jan	Design Example		
5	Mon	12-Jan	Verilog for Multi-Module Systems		HW4
	Tue	13-Jan	Verilog for Finite State Machines	8.3-8.5	Prelab 5
	Thur	15-Jan	Lab5		Lab 4
	Fri	16-Jan	System Simulation		
6	Mon	19-Jan	Clock Synchronization/More Asynchronous Inputs	10.3	HW 5
	Tue	20-Jan	**Exam 2**		PreDesign 1
	Thur	22-Jan	Begin Design Project		Lab 5
	Fri	23-Jan	CMOS Logic	3.1-3.3	
7	Mon	26-Jan	Transistor-Level Gates	3.1-3.3, 3.8.7	HW6
	Tue	27-Jan	Static (DC) Electrical Behavior, Noise Margin	3.8.2-3.8.4	PreDesign 2
	Thur	29-Jan	Continue work on design project		
	Fri	30-Jan	Dynamic (AC) Electrical Behavior	3.8.5, 3.8.6	
8	Mon	2-Feb	Other CMOS Input/Output Structures	3.8.7-3.9	HW7
	Tue	3-Feb	Other CMOS Input/Output Structures	notes	PreDesign 3
	Thur	5-Feb	Finish up design project		
	Fri	6-Feb	EMC and Signal Integrity	*EMC and Signal Integrity Resources*	
9	Mon	9-Feb	Transmission Line Effects	*Why Digital Engineers Don't Believe in EMC*	HW8
	Tue	10-Feb	Design for T-Line Effects		Prelab 9
	Thur	12-Feb	Lab 9		Design
	Fri	13-Feb	Simple Programmable Logic Devices (PLD's)	3.6.1, 3.6.2	
10	Mon	16-Feb	Memory (ROM,RAM)	10.1	HW9
	Tue	17-Feb	Complex PLDs and Field-Programmable	3.6.4, 3.10	Prelab 10
	Thur	19-Feb	Lab 10		Lab 9
	Fri	20-Feb	Gate Arrays (FPGAs)	3.6.5	
	Mon	23-Feb	**Final Exam**		To be scheduled