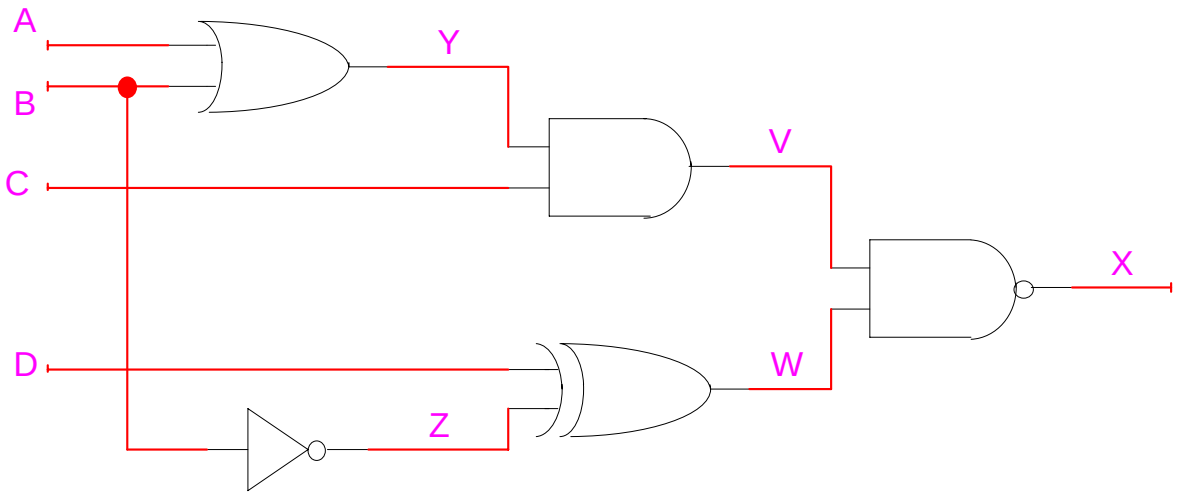
ECE 130 HW#7 – Due Friday, March 26

1. Consider the following circuit:



In this circuit, each gate has the following propagation delay:

Gate	Delay
inverter	1 ns
nand	2 ns
or	3 ns
and	3 ns
xor	4 ns

Complete the following timing diagram (each square is 1 ns):