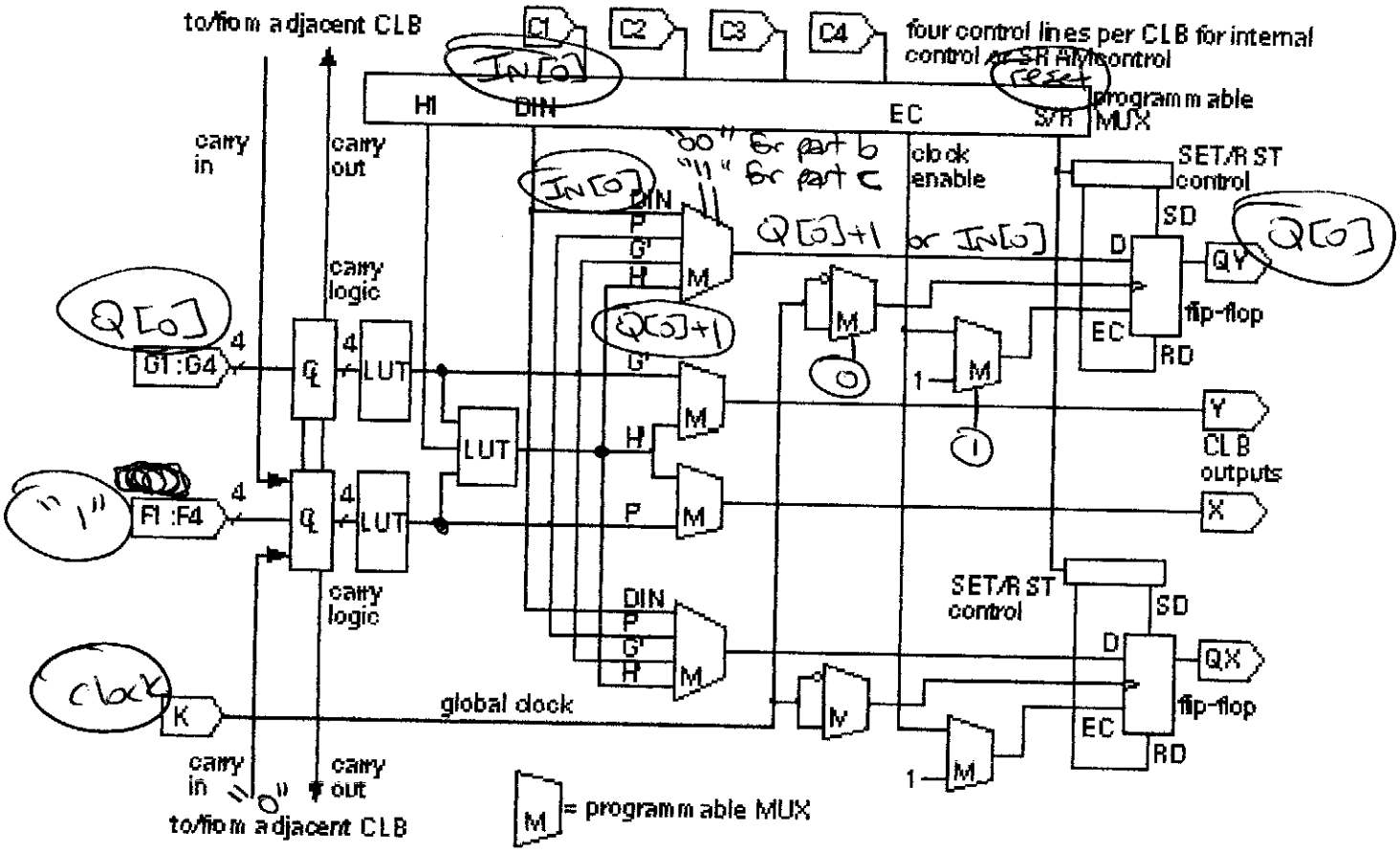
Homework 7 - Solutions [illegible]

Problem 1

The following diagram is the CLB for the Q[0] bit in the counter described by the verilog code below. You job it to determine how the CLB will be configured. to obtain the correct path for correct operation.

```
always @ (negedge clock and posedge reset)
   if (reset)
   Q<=4'b0000;
   else
   if (load ==1)
   Q<=In;
   else
   Q<=Q+1;
```



(a) How do the signals in the Verilog code map to the CLB? see diagram

(b) If the CLB is set to perform a load, what will the mux select lines be set to? Assume the top input to the muxes is the "0" input and the bottom input is the "1" or "11" input for the 2 or 4 input mux respectively See diagram. no hold, so EC = 1 always neg edge triggered so clock mux = 0

(c) If the CLB is set to count, what will the mux select lines be set to? See diagram: only 4-input mux changes to receive Q[0]+1 instead of IN[0]

Problem 2

Create a ROM for the following truth table.

Table 1:

Address	Bit1	Bit0
000	1	0
001	0	1
010	1	1
011	1	1
100	0	0
101	0	0
110	1	0
111	0	1