

# Homework 7 - Solutions Posted

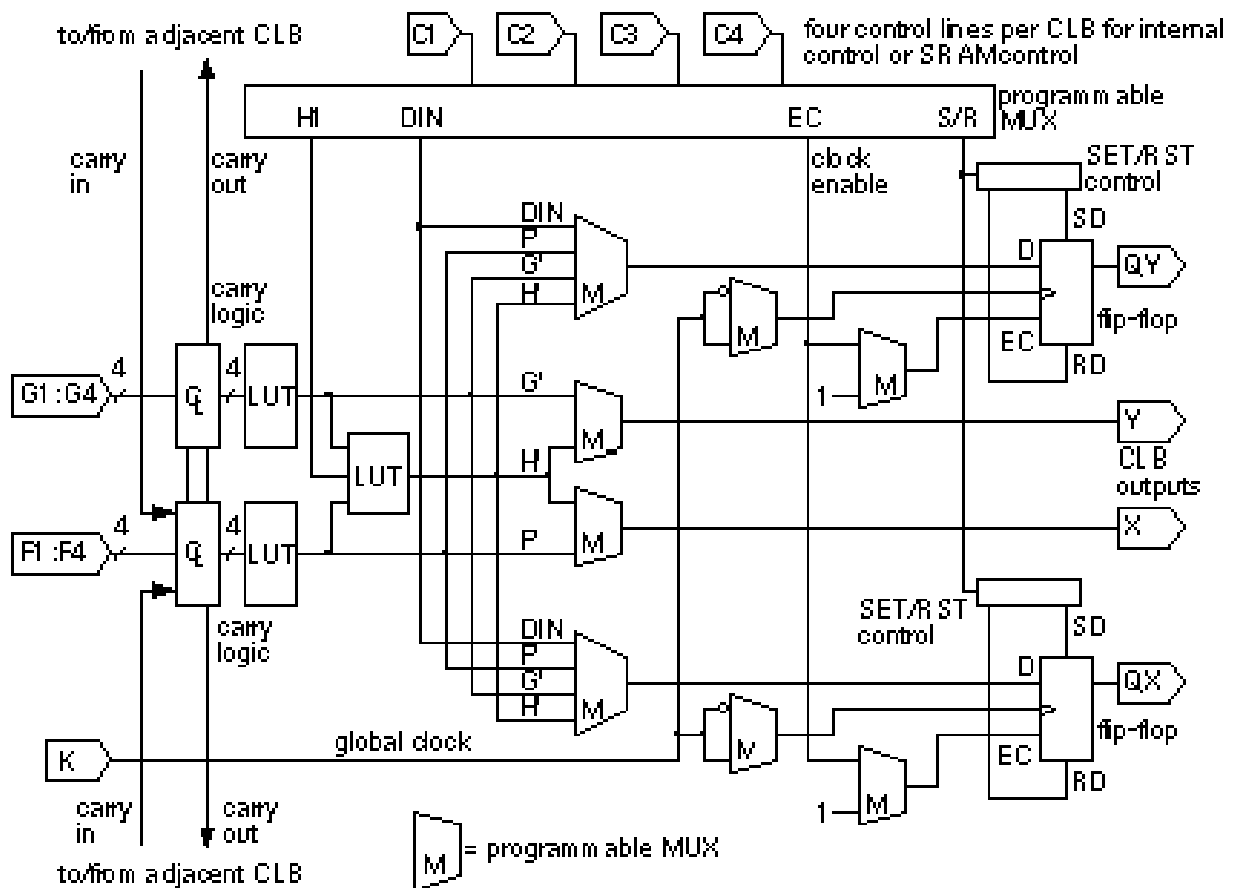
## Problem 1

The following diagram is the CLB for the Q[0] bit in the counter described by the verilog code below. Your job is to determine how the CLB will be configured to obtain the correct path for correct operation.

```

always @ (negedge clock and posedge reset)
  if (reset)
    Q<=4'b0000;
  else
    if (load ==1)
      Q<=In;
    else
      Q<=Q+1;

```



(a) How do the signals in the Verilog code map to the CLB?

(b) If the CLB is set to perform a load, what will the mux select lines be set to? Assume the top input to the muxes is the “0” input and the bottom input is the “1” or “11” input for the 2 or 4 input mux respectively

(c) If the CLB is set to count, what will the mux select lines be set to?

## Problem 2

Create a ROM for the following truth table.

**Table 1:**

Address	Bit1	Bit0
0 0 0	1	0
0 0 1	0	1
0 1 0	1	1
0 1 1	1	1
1 0 0	0	0
1 0 1	0	0
1 1 0	1	0
1 1 1	0	1