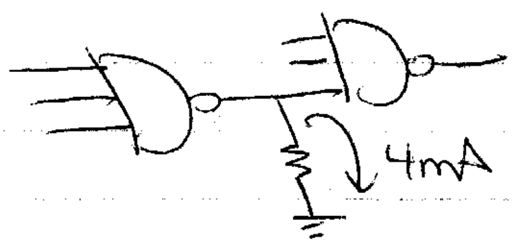
Homework 5 Solutions

Problem 1:

a)



high state NM = $V_{OH} - V_{IH}$

V_{OH} will source 4mA,

so from data sheet,

worst case V_{OH} w/ 4mA load @ 4.5V supply

= 3.7V

$V_{IH} = 3.15V$

high state NM = 3.7 − 3.15 = 0.55V

low state NM = $V_{IL} - V_{OL}$

when $V_{out} = 0$, no I sourced, so

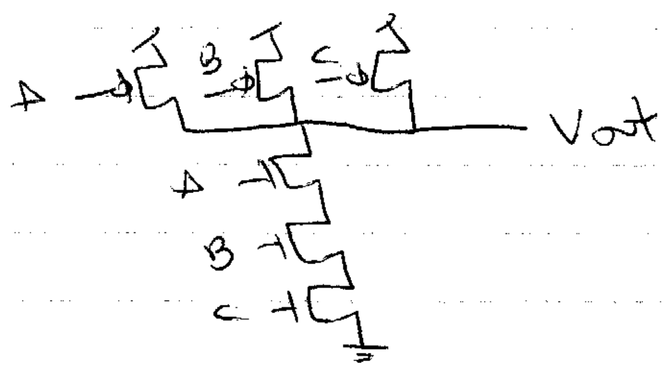
$V_{OL} = 0V$

$V_{IL} = 1.35$

low state NM = 1.35 − 0 = 1.35V

b) assuming gate is sinking or sourcing 4mA,
worst case $V_{OL} = 0.4V$
worst case $V_{OH} = 3.7V$

3-input NAND gate looks like:

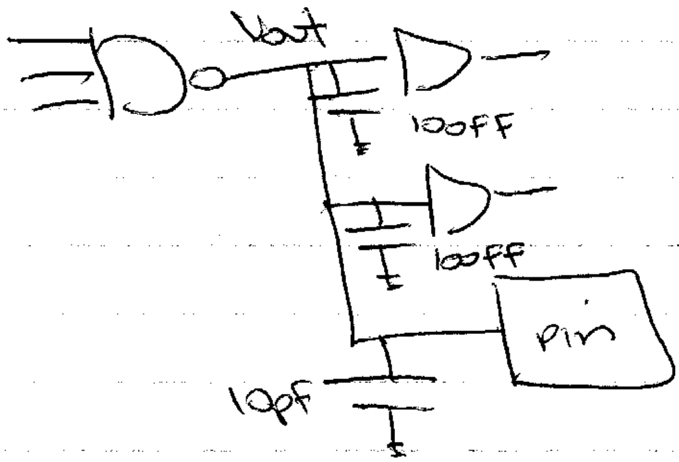


If $R_{dsN} = R_{dsP} = 10\Omega$ as we have previously assumed, $V_{OL} > V_{DD} - V_{OH}$ because R_{dsN}'s would add in series

however, as shown above, $V_{OL} = 0.4 < V_{DD} - V_{OH} = 0.8V$

therefore, $R_{dsN} < R_{dsP}$

Problem 2:



Fall time assumes Vout starts at Vdd & falls to zero
⇒ nFET network discharges equivalent cap at Vout

$t_{fall} \simeq 2.2\,RC$

$C = 100fF + 100fF + 10pF$

$R = (10\Omega)3$ — 3 nFETs in series

$t_{fall} \simeq 2.2(30\Omega)(10.2fF)$

$t_{fall} \simeq 673.2\ psec$

Problem 3

$$P_T = (C_L + C_{PD}) \cdot V_{DD}^2 \cdot f$$

same device, only dropping V_{DD}, so C_L & C_{PD} & f are the same for both calc.

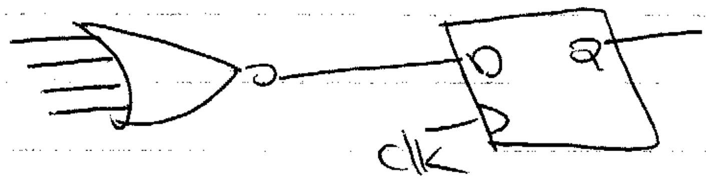
$$P_{T6} = (6)^2 [(C_L + C_{PD}) f]$$
$$P_{T2V} = (2)^2 [(C_L + C_{PD}) f]$$

$$\% \text{ diff} = \frac{(36-4)\,[\cancel{(C_L + C_{PD}) f}]}{36\,[\cancel{(C_L + C_{PD}) f}]} \times 100$$

$$= 88.89\% \text{ savings}$$

Problem 4

A)



$V_{IL} = 0.8V \quad V_{IH} = 2.2V$

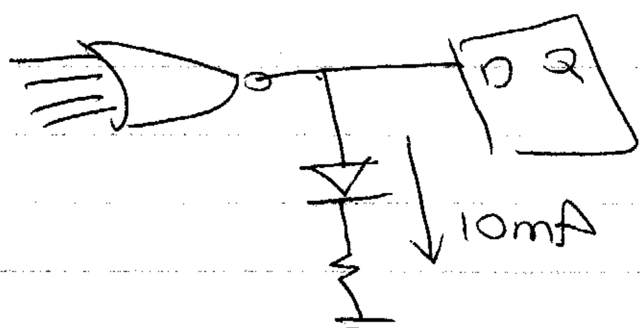
purely capacitive load so

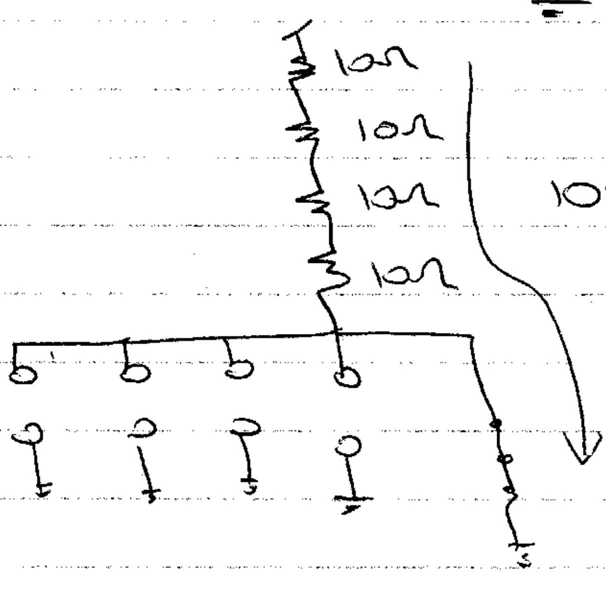
$V_{OH} = V_{dd} = 3.3V$

$V_{OL} = 0V$

high state NM $= V_{OH} - V_{IH} = 3.3 - 2.2 = 1.1V$
low state NM $= V_{IL} - V_{OL} = 0.8 - 0 = 0.8V$

B)

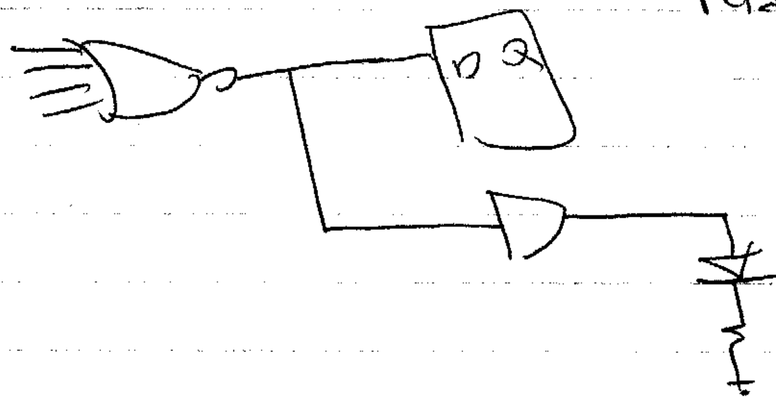




$V_{OH} = V_{DD} - (10mA)(40\Omega)$
$= 2.9$

high state NM $=$
$2.9 - 2.2 = 0.7V$
low state NM doesn't change
$= 0.8V$

c) NAND would see buffer instead of LED, so it would retain its capacitive load.



As a consequence, the high state NM would be improved (equal to part (a)).