

Homework 5

Problem 1

- (a) Find the worst case high and low state noise margin for the triple 3-input NAND gate used in lab1. Assume a 3-input NAND gate is driving another 3-input NAND gate and a resistive load that requires 4mA. The power supply for the system is set to 4.5V.
- (b) What do the values used in part (a) tell you about the R_{ds} values of the pFETs in this gate verses nFETs?

Problem 2

A 3-input NAND gate is driving 2 buffers and an output pin. If the output pin = 10pF and the input capacitance of each buffer is 100fF, what is the fall time for the gate? Assume $R_{ds}=10\Omega$.

Problem 3

The data sheet for the 3-input NAND gate used in lab 1 indicates that the device can be used at either 6V or 2V. If the gate is driving the same load at the same frequency, what would the power savings be if the gate used the 2V power supply as opposed to the 6V power supply?

Problem 4

You have designed a circuit that contains a 4-input NOR gate driving a flip-flop and programmed the Xilinx board with this circuit.

- (a) If V_{IL} for the flip-flop is 0.8V and V_{IH} is 2.2V, find the low and high state noise margin for the circuit. Assume the Xilinx chip uses CMOS gates. $V_{dd}=3.3V$ on the Xilinx board.
- (b) To test your circuit operation, you decide to use the internal node between the NOR gate and the flip-flop to drive the LEDs on the IO board. The LEDs require 10mA to operate. Calculate the new noise margin. Assume $R_{ds}=10\Omega$. (Check the I/O board schematic to see how the LEDs are connected.)
- (c) Typically, the Xilinx software adds a buffer for any internal node that drives an output pin. Explain how this would help the problem presented in part (b).