

**ECE 333 - Digital Systems**  
Tentative course schedule - Fall 2003

Week	Day	Date	Topic	Reading	Due Dates
0	Thur	4-Sep	Course Overview	Chapt 1	
1	Mon	8-Sep	Review Digital Logic: Combinational Circuits	2.1-2.8,4.1-4.5 & 5.3,6.1,6.2,6.5	Prelab 1 due
	Tues	9-Sep	Review Digital Logic: Sequential Circuits, finite state machines	7.1-7.6,7.8,7.9 & 8.1-8.3, 8.7	
	Wed	10-Sep	Lab 1		
	Thur	11-Sep	Verilog HDL	2.1	HW1 due
2	Mon	15-Sep	Combinational Circuits	<i>Gradual Intro to Verilog: Combinational</i> , & 6.6 class demo	Prelab 2/Lab 1 due HW2 due
	Tues	16-Sep	Simulation Techniques for Combinational Circuits		
	Wed	17-Sep	Lab2		
	Thur	18-Sep	Sequential Circuits	<i>Gradual Intro to Verilog: Sequential</i> & 7.12-7.14 class demo	
3	Mon	22-Sep	Simulation Techniques for Sequential Circuits		Prelab 3/Lab 2 due
	Tues	23-Sep	<b>Exam 1</b>		
	Wed	24-Sep	Lab3		
	Thur	25-Sep	Handshaking Between FSMs and Asynchronous Inputs	10.3.3	
4	Mon	29-Sep	Data Path/Controller Partion	10.2	Prelab 4 due Lab 3 due HW3 due
	Tues	30-Sep	Design Example		
	Wed	1-Oct	Lab4		
	Thur	2-Oct	Verilog for Multi-Module Systems		
5	Mon	6-Oct	Verilog for Finite State Machines	8.3-8.5	Prelab 5 due Lab 4 due HW 4 due
	Tues	7-Oct	System Simulation		
	Wed	8-Oct	Lab5		
	Thur	9-Oct	Clock Synchronization/More Asynchronous Inputs	10.3	
6	Mon	13-Oct	<b>Exam 2</b>		Prelab Design Project Due Lab 5 due
	Tues	14-Oct	CMOS Logic	3.1-3.3	
	Wed	15-Oct	Begin Design Project		
<b>Break</b>					
7	Mon	20-Oct	Transistor-Level Gates	3.1-3.3, 3.8.7	HW5 due
	Tues	21-Oct	Static (DC) Electrical Behavior, Noise Margin	3.8.2-3.8.4	
	Wed	22-Oct	Continue work on design project		
	Thur	23-Oct	Dynamic (AC) Electrical Behavior	3.8.5, 3.8.6	
8	Mon	27-Oct	Other CMOS Input/Output Structures	3.8.7-3.9	HW6 due
	Tues	28-Oct	Other CMOS Input/Output Structures	notes	
	Wed	29-Oct	Finish up design project		
	Thur	30-Oct	EMC and Signal Integrity	<i>EMC and Signal Integrity Resources</i>	
9	Mon	3-Nov	Transmission Line Effects	<i>Why Digital Engineers Don't Believe in EMC</i>	Prelab 9 Due Design Project Due HW7 due
	Tues	4-Nov	Design for T-Line Effects		
	Wed	5-Nov	Lab 9		
	Thur	6-Nov	Simple Programmable Logic Devices (PLD's)	3.6.1, 3.6.2	
10	Mon	10-Nov	Memory (ROM, RAM)	10.1	Prelab 10 Due  Lab 9 due HW8 due
	Tues	11-Nov	Complex PLDs and Field-Programmable Gate Arrays (FPGAs)	3.6.4, 3.10 3.6.5	
	Wed	12-Nov	Lab 10		
	Thur	13-Nov	Applications		
finals week			<b>Exam 3</b>		Lab 10 due Monday of finals week

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build hardware using discrete parts

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combinational verilog (GAL)

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sequential verilog (GAL)

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comb verilog (FPGA)

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system verilog (FPGA)

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design project

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